



CST5080A OTP-type Speech IC

1. CST5080A General Descriptions

CST5080A series are 4-bits micro-controller which could play 4 channel melody or 4 channel ADPCM with PWM direct drive circuit. PWM resolution is 8/10/12 bits. They includes a low cost, high performance CMOS micro-processor. The clock frequency of this up is typically 8.192 ($\pm 3\%$) MHz. This chip operates over a wide voltage range of 2.0V~5.5V. It contains program ROM (PROM) and data ROM (DROM) inside. The program ROM is 8K words and data ROM size is 240K byte. The maximum working SRAM is (128+2) nibbles. It is provided with total 12 software programmable I/O Ports.

2. CST5080A Features

- Operating voltage: **2.0V to 5.5V**
- MCU Operation frequency: **8.192MHz**
- Memory Size
 - Program ROM size: **8K*12-bits OTP type**
 - Data ROM size: **240K*8-bits OTP type**
 - SRAM size: **128*4 bits**
 - User register: **2*4 bits**
- Wakeup function for power-down mode:
 - HALT mode wakeup source: Port A, Port B and Port E/CE can wake-up from HALT mode to NORMAL mode and executing wake-up sub-routine program.
- 8 input/output pins: Port A and Port B can be defined as input or output port bit by bit.
- 4 input/output ports or 4 input only ports or 4 output only ports "Port CE/E/C" defined by option:
 - If input only ports are employed, Port E defined as input only ports.
 - If output only ports are employed, Port C defined as output only ports.
 - If input/output ports are selected, Port CE defined as input/output ports bit by bit.
- Four reset condition:
 - Low voltage reset. (LVR = 2.0V)
 - Power on reset.
 - External reset pin. (active low)
 - Watch dog timer overflow.
- One internal interrupt sources:
 - PWM interrupt.
- WDT
 - Watch dog timer, can enabled/disabled by option.
 - WDT period is $256*256*16/F_{sys}$. (WDT period is 0.13 sec for system clock=8.192MHz)
- Audio output:
 - Support PWM or DAC mode by option.
 - Support 8/10/12 bits.
- Support option set for pull down resistor 1M, 50K or 220K Ohm, reset pin (PB3 or PC3), low voltage reset...etc.
- Oscillator fuse option **$\pm 3\%$, temperature & voltage compensation.**
- Support **security option (1 bit)** for read inhibition.
- Support 16-levels LVD function.



CST5080A OTP-type Speech IC

The I/O ports, RAM, ROM sizes and functions table of CST5080A are shown below :

Body	CST5080A	CST5080A
Voice duration	80 sec.	
RAM size	(128+2)*4-bits	
I/O pins	12 I/O 8 I/O + 4I 8 I/O + 4O	
PROM size	8K*12-bits	
DROM size	240K*8-bits	

3. CST5080A Packaging and Pads Information

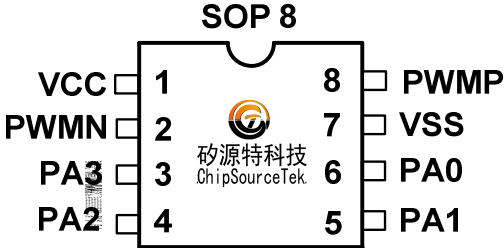
3.1 Pads

PAD Name	Type	After Reset	Description
VCC	P	High	Power input of I/O port.
VSS	P	Low	Ground input except PWM block power. It could be double bonded with VPS pad.
VPD	P	High	PWM block power input in normal operation.
VPS	P	Low	The ground pad of PWM block. It could be double bonded with VSS pad.
PA3~PA0	I/O	zzzz	Port A is a programmable input/output port.
PB3~PB0	I/O	zzzz	Port B is a programmable input/output port. PB3 can be employed as reset pin according to the option.
PE3~PE0	I	zzzz	Port E is an input only port defined by option.
PC3~PC0	O	0000	Port C is an output only port defined by option, PC3 can be employed as reset pin according to the option.
PCE3~PCE0	I/O	zzzz	Port CE is a programmable input/output port defined by option, PCE3 can be employed as reset pin according to the option.
PWMP	O	Low	Audio output PWM(+).
PWMN	O	Low	Audio output PWM(-).

Table 1: Pad Description

3.2 Package

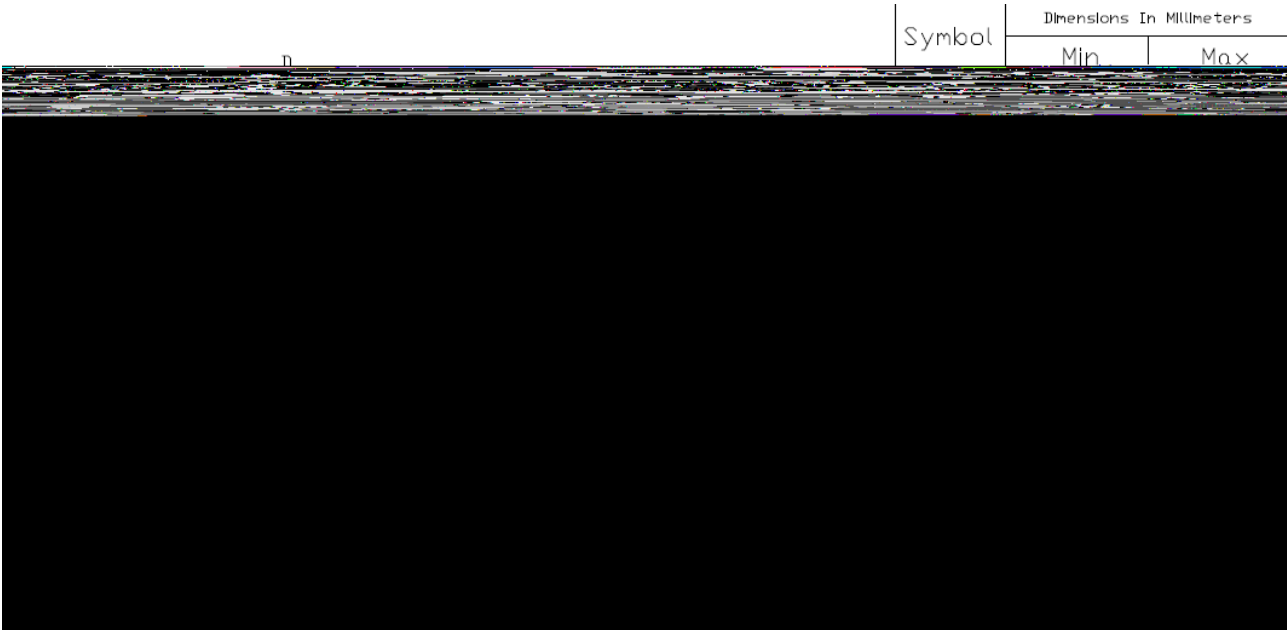
CST5080A provides SOP8 and SOP16





CST5080A OTP-type Speech IC

3.2.2 SOP16



3.3 Block Diagram

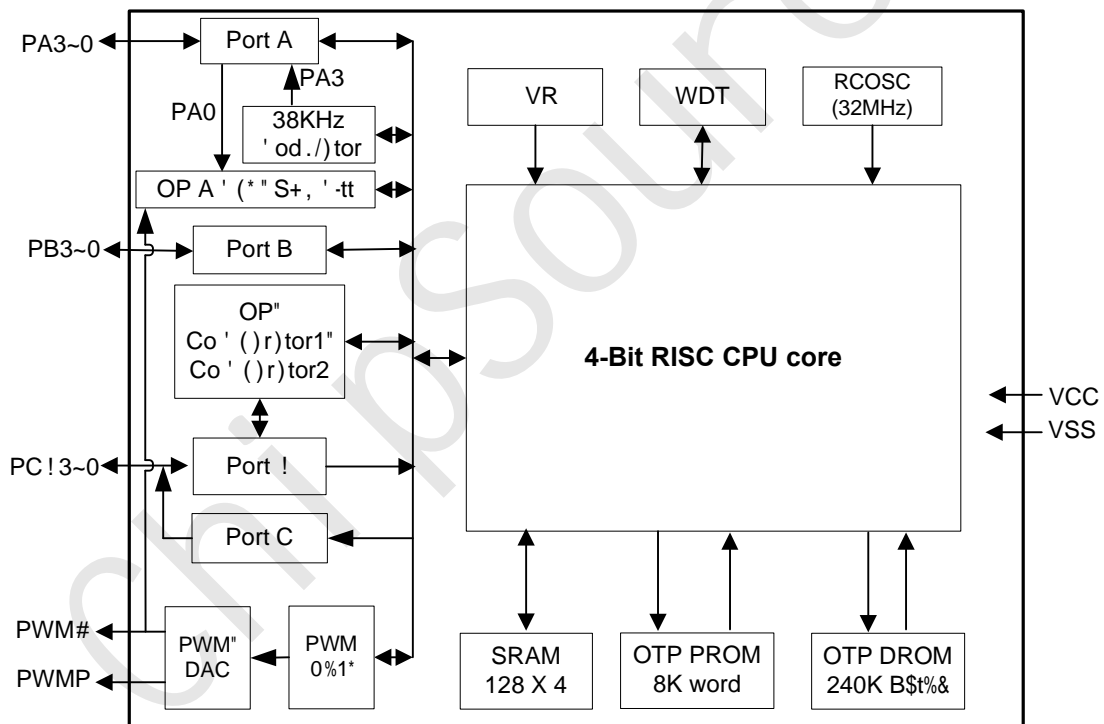


Figure1. Block diagram



CST5080A OTP-type Speech IC

4. CST5080A ELECTRICAL CHARACTERISTICS

4.1 Absolute Maximum Ratings

Parameters	Symbol	Value	Unit
DC Supply Voltage	V _{cc}	-0.5 to 6.0	V
Input Voltage	V _{in}	-0.5 to V _{cc} +0.5	V
Operating Temperature Range	T _a	0 to +75	°C
Storage Temperature Range	T _{stg}	-25 to +85	°C

Table 2: Absolute Maximum Ratings

4.2 AC Characteristics

V_{CC}=3.0V, T_a=25°C unless otherwise noted.

Parameters	Symbol	Minimum	Typical	Maximum
Operating Frequency(RC Oscillator)	F _{sys}	7.946MHz	8.192 MHz	8.43MHz
RC reset time-constant	T _{rrc}	-	10 us	-
Data ROM data ready time	T _{drr}	-	-	2/F _{sys}

Table 3: AC Characteristics

4.3 DC Characteristics

VCC=3.0V, Ta=25°C unless otherwise noted.

Parameters	Symbol	Minimum	Typical	Maximum	Condition
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CST5080A OTP-type Speech IC

PROM address	Function description
0x0000 ~ 0x0001	Reset
0x0004 ~ 0x0005	Wake-up
0x0008 ~ 0x0009	Interrupt
0x000A ~ 0x1EFF	User code of CST5080A
0x1F00 ~ 0x1FFF	Reserve area of CST5080A

Table 3: Memory Map of PROM

5.2 Data ROM (DROM)

The DROM is an OTP (One Time Programmable) type memory. The maximum **DROM is 240K*8-bits** which stores the 8-bits wide data for ADPCM or melody data ...etc. The last 64 location is a reserved area. The user shall not use this area in any case. Assembler shall check user data ROM on this limit. Hardware does not need to check this restriction.

DROM address (DMA)	Function description
0x00000 ~ 0x000FF	User area
0x00100 ~ 0x001FF	User area
0x00200 ~ 0x002FF	User area
...	...
0x3BFB0 ~ 0x3BFBF	User area (Max. size of CST5080A)
0x3BFC0 ~ 0x3BFFF	System area, last 64 location(don't use it)

Table 4: Memory Map of DROM

DROM is addressed by five registers DMA4, DMA3, DMA2, DMA1 and DMA0. After these registers are specified by software, the data need enough delay time, T_{dr} in the table of "AC Characteristics". After this delay time, the data can be read from data register (DMDL & DMDH).

Ex:

```
LD    (DMA0), A
...
LD    (DMA4), A    ; Set DMA0~4
LD    A, (DMDL)   ; Read low nibble data from DROM, address as DMA4~0.
LD    A, (DMDH)   ; Read high nibble data from DROM, address as DMA4~0.
```

Symbol	Addr	type	Reset	D3	D2	D1	D0	Description
DMA0	18H	R/W	xxxx	DMA0.3	DMA0.2	DMA0.1	DMA0.0	DMA0~4, five register built a 20-bits addressing space for read DROM 8-bits data.
DMA1	19H	R/W	xxxx	DMA1.3	DMA1.2	DMA1.1	DMA1.0	
DMA2	1AH	R/W	xxxx	DMA2.3	DMA2.2	DMA2.1	DMA2.0	
DMA3	1BH	R/W	xxxx	DMA3.3	DMA3.2	DMA3.1	DMA3.0	
DMDL	1CH	R/W	xxxx	DMDL.3	DMDL.2	DMDL.1	DMDL.0	Low nibble of DROM data read from this address.
DMDH	1DH	R/W	xxxx	DMDH.3	DMDH.2	DMDH.1	DMDH.0	High nibble of DROM data read from this address.
								this timer is enabled by option.
DMA4	1EH	R/W	xxxx	-	-	DMA4.1	DMA4.0	DMA4 is highest nibble of DROM address

Table 5: SFRs about DROM

5.3 SRAM and Special Function Register

5.3.1 SRAM

There are 128 nibbles SRAM in this chip. The SRAM and I/O memory map is divided into several pages by setting MAH register (2-bits wide). The initial value of MAH is unknown and must be defined by instructions “LDMAH” before you utilize SRAM. The extra 2 SRAM nibbles in the specifications and hardware manuals of relative mask ROM products are not SRAM in fact. They are USER1 and USER2 of SFRs.

Direct Addressing		SRAM MAP
MAH=XH	00H~1FH	SFR(special function register) register
MAH=0H	20H~3FH	USER SRAM
MAH=1H	20H~3FH	
MAH=2H	20H~3FH	
MAH=3H	20H~3FH	

Table 6: Memory Map of SFRs

The first 32-nibble, 00H ~ 1FH, are defined as a common block. Some I/O and user register is arranged in this common block for easy data operations. The other regions, 20H~3FH, are employed as SRAM. The user must notice that the initial content of SRAM is unknown.

5.3.2 Special Function Registers

The special function register consists of common I/O and other special register.

A special function register supports LD/ADC/SBC/OR/AND/XOR/INC/DEC/RLC/RRC/CMP/ADR operation. Bit set/clear can only be operated on the address range from 00H to 0FH, except indirect operation is used.

The following table describes all of the SFRs.

Symbol	Addr	R/W type	Reset	D3	D2	D1	D0	Description
--------	------	----------	-------	----	----	----	----	-------------

LVD_CTRL	13H	R/W	0000	-	-	LVD_FLAG (R)	LV DEN	LVD_FLAG: (Read only) The flag of LVD, '1'=LVD sensing. LV DEN: '1'=Enable LVD function, '0'=Disable LVD function.
LVDS	14H	R/W	0000	LVDS3	LVDS2	LVDS1	LVDS0	LVDS[3:0]: LVD level selected, 1111=3.8V, 1110=3.7V, 1101=3.6V, 1100=3.4V, 1011=3.3V, 1010=3.2V, 1001=3.1V, 1000=3.0V, 0111=2.9V, 0110=2.8V, 0101=2.7V, 0100=2.5V, 0011=2.4V, 0010=2.3V, 0001=2.2V, 0000=2.1V.
Reserved	15H~ 17H	-	xxxx					

When interrupt service routine is done, an RETI shall be executed. This instruction will restore stored program counter, PCDH, MAH and C/Z, will set interrupt enable bit=1 also. (Note that RETI is different from RETS.) Interrupt request can be accepted only when enable bit be set. Note that only one level of INT routine can be used.

5.6 Clock Operation

There are two operation modes in this chip. The state diagram of three MCU operation modes is shown below:

1. NORMAL Mode: In normal mode, system clock oscillator is running, and MCU clock source is come from main oscillator. In NORMAL mode, MCU will go to halt mode after HALT instruction executed.

2. HALT Mode: In HALT mode, the MCU clock stops, users can't change the operation mode when in halt mode. It will go back to NORMAL mode (Program counter=0x0004) when I/O wakeup or reset occurred. Please refer to the section of "Halt Mode & Wake up" for the detailed HALT mode description.

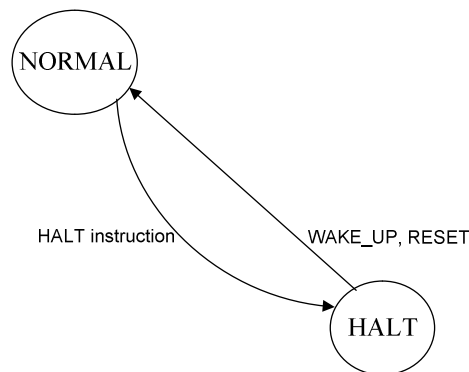


Figure 2: Clock Operation Mode

5.7 Halt Mode & Wake up

The MCU is changed into HALT mode (program counter and system clock stop) when HALT instruction executed. It provides a power saving mode for those applications requiring a very low stand-by current. The PA[3:0], PB[3:0] and PE[3:0] are supporting the wake-up function when rising edge occurred.

The program counter will be 0x0004 when HALT instruction executed immediately, then program counter will go to next address after 64 stable clock(system clock) when wake up condition occurred. Reset signal will release HALT state and execute reset procedure because reset is first priority when in HALT mode, so program counter will from 0x0004 to 0x0000, program counter goes to next address after 64 stable clock cycles. Furthermore, the SRAM will keep their previous data without changing in this mode.

5.8 Watch Dog Timer Reset (WDT)

The **Watch Dog Timer (WDT)** is used to reset whole chip when detect unexpected execution sequence caused by accident condition, avoiding dead lock of MCU program. WDT will be reset when wake-up from halt, after reset or software clears it. The watch dog timer is a simple counter. It has a fixed length of **256*256*16/system-clock (ex: 0.13 sec for 8.192MHz system clock)** after the clearance of watch dog.

Software must run a "clear watch dog timer" (

assembler will generate a warning (program code will still be generated). "HALT" instruction will reset watch dog timer. The reset watch dog timer sequence is strongly recommended as:

```
WATCHDOG:
        LD      (1DH), A
```

5.9 Low Voltage Detect (LVD)

The low voltage detect (LVD) function is used to detect whole chip power supply VCC. CST5080A support



CST5080A OTP-type Speech IC

								The low nibble of 8-bits PWM. The bit5~2 of 10-bits PWM. The bit7~4 of 12-bits PWM.
AUD_DH	OBH	W	XXXX	AUD_DH3	AUD_DH2	AUD_DH1	AUD_DH0	AUD_DH[3:0]: The high nibble of 8 bits PWM. The bit9~6 of 10 bits PWM. The bit11~8 of 12 bits PWM. Note: AUD_DH3 is sign bit, "0" means positive.

Table 10: SFRs about the operation of PWM

5.10.1 8-Bits PWM/DAC

This PWM is 8-bits output resolution. An interrupt request happened when a PWM cycle completed.

The MSB of AUD_DH is signed bit, '0' for positive, '1' for negative. PWM output frequency (sample rate) is fixed at 32KHz. PWM data registers are AUD_DL, AUD_DH. The AUL_DL is low nibble (D3 ~ D0). AUD_DH is high nibble (D7 ~ D4). D7 is the signed bit and D6 ~ D0 is the length (clock number) of output active pulse. Software should write AUD_DL and AUD_DH before enable PWM.

When an interrupt request happened, PWM interrupt flag bit PWFG of STATUS register will be "1". The PWM will load previously-written-data into actual conversion port on end of a PWM code output. So program can write data into PWM data store safely at beginning of an interrupt service routine. (A PWM interrupt means PWM data loaded, next data is expected). This timing shall be controlled carefully such that data writing in the beginning of interrupt service routine is safe. If data is not changed during a conversion, previous data will be used.

This PWM output can drive 8 ohm speaker. PWM can be enabled or disabled by setting/clearing ENPWM of PWM_CTRL. When disabled, the PWMP, PWMN pins are all '0'. "HALT" instruction will disable PWM (clear ENPWM of PWM_CTRL) and the PWMP and PWMN pins will be tri-state.

5.10.2 10-Bits PWM/DAC

The frequency of PWM clock is fixed at 32 KHz if 10-bits PWM mode is selected by option. The 10-bits PWM data (AUD_DH[3:0], AUD_DL[3:0], AUD_DLL[3:2]) are consist of AUD_DH, AUD_DL, AUD_DLL three registers shown above. The data rage is 0 ~511. Software should write these registers before PWM is enabled. The other features of 10-bits PWM is the same as 8-bits PWM.

5.10.3 12-Bits PWM/DAC

The frequency of PWM clock is fixed at 32 KHz if 12-bits PWM mode is selected by option "PWM12S". The 12-bits PWM data (AUD_DH[3:0], AUD_DL[3:0], AUD_DLL[3:0]) are consist of AUD_DH, AUD_DL, AUD_DLL three registers shown above. The data rage is 0 ~ 2047. Software should write these registers before PWM is enabled. The other features of 12-bits PWM is the same as 8-bits PWM.

Note: To avoid sound "Bo", please reference application note on TRITAN web site.

5.10.4 Speaker Provided a Wake-up Control Function

Normally, the PWMN and PWMP pin is tied to a speaker for playing music and a sound. This speaker connection structure can be used to wake-up MCU. If PWMWK is enabled, the speaker wake-up function is enabled after go into HALT mode and the PWM function keep operating in normal mode. If speaker wake-up function is enabled, the PWMP pin will be fixed to VSS level and PWMN pin also will be fixed to VSS level by chip. The signal level on PWMN pin will be changed (typically 0mV~10mV) when a sound receives



CST5080A OTP-type Speech IC

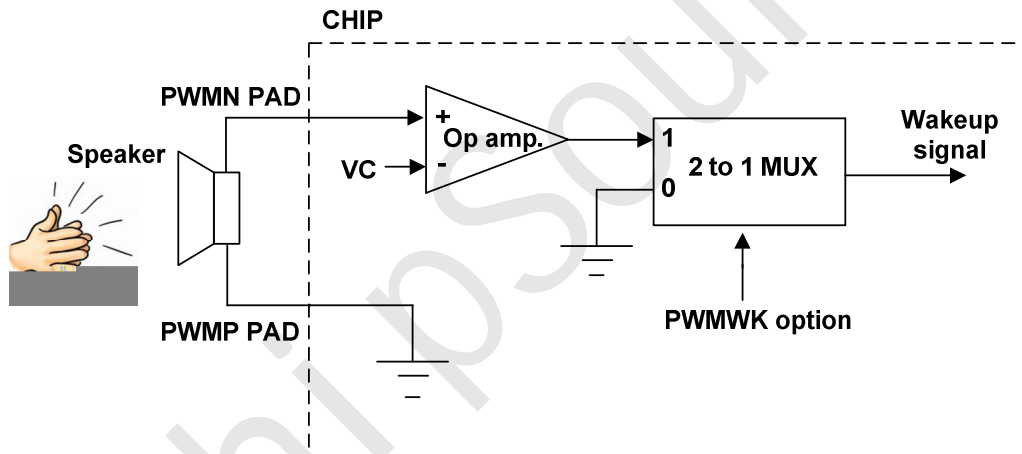
from speaker. The MCU will be waked up if signal level on PWMN pin high enough. The relationship between wake-up signal and PWMN pin is shown in picture below. The wake-up signal goes high if PWMN pin larger than VC level and it goes low if PWMN pin smaller than VC level.

Note:

1. This function consume about 5uA (VDD=5V) typically in HALT mode when “PWMWK” option is enabled.
2. PWM function must be keep silence about 200ms before go into HALT mode. Otherwise, MCU maybe keep in normal mode, not goes into HALT mode.
3. When PWMWK option enabled, PA0 wakeup option must be disabled, please referenced AN-0068_V2.0.
4. If ENGAIN enabled, option OPEN function should be disable.

Symbol	Addr	R/W type	Reset	D3	D2	D1	D0	Description										
PWMWK	12H	R/W	0000	PWMWCFG	CLAPSEL1	CLAPSEL0	PWMWKEN	<p>PWMWCFG : When wakeup source form Speaker, it will be set by hardware, it could be clear by software.</p> <p>PWMWKEN: Wakeup by speaker. 1: Enable PWM wakeup function. 0: Disable PWM wakeup function.</p> <p>CLAPSEL[1:0]: Sensitivity of speaker wakeup.</p> <table border="1"> <thead> <tr> <th>CLAPSEL[1:0]</th> <th>Sensitivity</th> </tr> </thead> <tbody> <tr> <td>00</td> <td>Level 1 (low)</td> </tr> <tr> <td>01</td> <td>Level 2</td> </tr> <tr> <td>10</td> <td>Level 3</td> </tr> <tr> <td>11</td> <td>Level 4 (High)</td> </tr> </tbody> </table>	CLAPSEL[1:0]	Sensitivity	00	Level 1 (low)	01	Level 2	10	Level 3	11	Level 4 (High)
CLAPSEL[1:0]	Sensitivity																	
00	Level 1 (low)																	
01	Level 2																	
10	Level 3																	
11	Level 4 (High)																	

Table 13: SFRs about the operation of speaker wakeup function

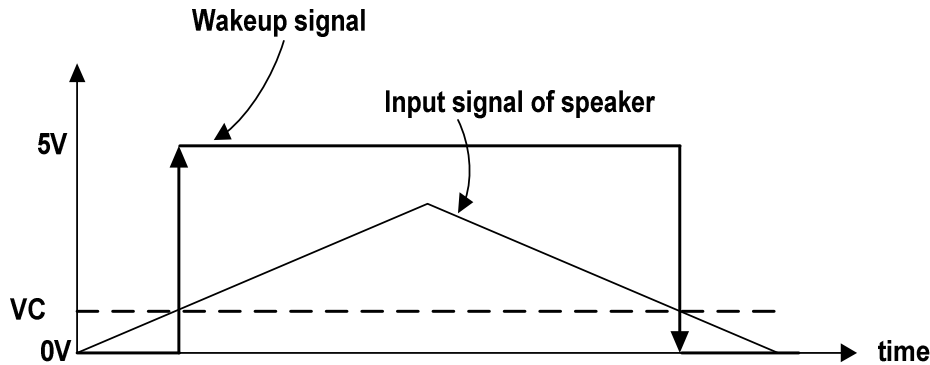


Wakeup control block diagram and speaker trigger application circuit

Figure 3: Speaker wakeup structure



CST5080A OTP-type Speech IC



Input signal of speaker vs. Wakeup signal waveform

Figure 4: Speaker wakeup waveform

Notice: Speaker wakeup function, please reference application note “AN-0068_V1.0” on TRITAN web site.

5.11 Reset Function

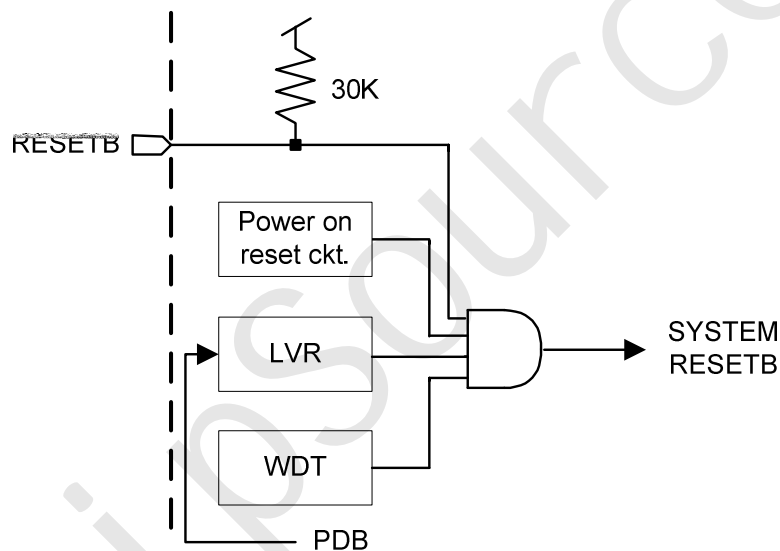


Figure 5: Reset structure

The system reset is come from four signals which are **Power on reset**, **Low voltage reset(LVR)**, **External RESETB pin** and **WDT overflow reset**.

Some reset input pins PB3 and PC3, can be provided to reset this chip according to your option. These pins have 30K Ohm pull up resistor. For normal operation of this chip, a good reset is needed. The operation frequency of MCU will go back to normal mode when reset occurred in HALT mode.



CST5080A OTP-type Speech IC

5.12 System Clock Oscillator

This chip MCU is typically operated on 8.192MHz which is generated from internal RC oscillator 32MHz.

5.13 I/O Ports

There are three I/O ports, PA3~PA0, PB3~PB0 and PE3~PE0, whose input/output direction are defined by IOC_PA, IOC_PB and IOC_PCE. PE3~PE0 are input only ports or input/output ports direction defined by IOC_PCE be selected by option. The wake-up functions of PA3~PA0, PB3~PB0 and PE3~PE0 are enabled or disabled by option. All I/O ports provides rising or falling edge wake up function. This double edge wake up function can be enabled by "BIWK" option. Their 1M/50K Ohm pull down resistors are optional.

In order to achieve touch function, CST5080A support 220K Ohm pull down resistors. These resistors can be enabled by using 50K Ohm pull down resistor registers after "PD220K" is enabled. The 220K Ohm resistance value is almost fixed value when VCC change from 2.0V to 5.5V.

5.13.1 Port PA (input/output)

The Port A is 4-bits bidirectional I/O port. Their directions can be defined by IOC_PA bit by bit. The following table describe the SFRs associated with Port A.

Symbol	Addr	R/W type	Reset	D3	D2	D1	D0	Description
IOC_PA	02H	R/W	0000	IOCA3	IOCA2	IOCA1	IOCA0	"1" = output, "0" = input of related PA bit.
DATA_PA	03H	R/W	xxxx	DPA3	DPA2	DPA1	DPA0	Read from Port A input port and write to output port.

Table 14: SFRs of Ports PA

In output mode, the data can be written out to external pin, and reading this output port will read the data internal latch. Pull-down resistor will be disabled when output mode is selected.

In input mode, Port A and Port B data can be read from external pin, and they are attached with 1M/50K Ohm pull-down resistor or not according to the options.

In addition, each pin of Port A and Port B also can be accompanied with wake-up function according to the options. In HALT mode, if some bits of Port A or Port B are accompanied with wake-up function, any rising edge occurred on that pin will wake up system and turn on oscillator, and the program counter of MCU will jump to the address 0x0004. This device will start to execute the wake-up sub-routing.

PA3 is provided with 38KHz modulator

I/O port PA3 built-in a 38KHz modulator combined with register DATA_PA bit-3, this function is enabled by "F38K" option. If F38K option is enabled, I/O port PA3 will output 38KHz clock signal when PA3 is configured as output port and DATA_PA bit-3 = 1. PA3 output low when PA3 is configured as output port and DATA_PA bit-3 = 0.

Notice: The PA3 output pad will be forced to low state automatically by hardware control when in halt mode for avoid external IR LED destroyed. Besides, the F38K option disabled, PA3 is a normal I/O port.

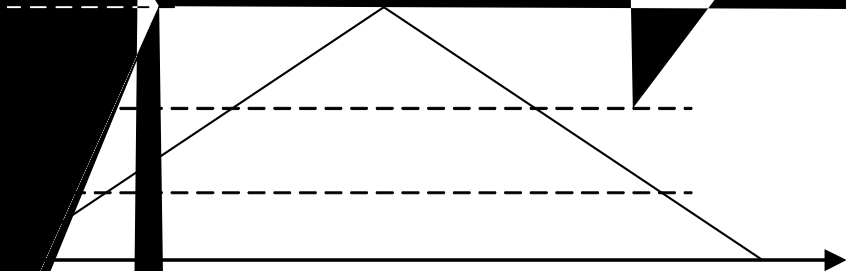
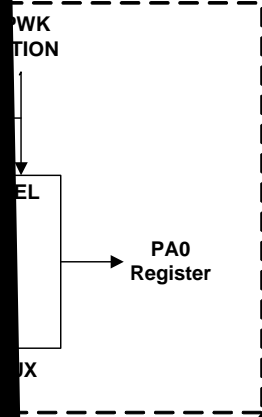
PA0 is provided with an analog input (Schmitt) for wake-up control

PA0 supports an analog input buffer with Schmitt circuit, it is enabled by "RCWK" option and supports low power consumption in halt mode, if PA0 analog signal keep about 0.5*VCC, so this function is suitable for recycle wakeup MCU by external RC time constant, external RC time constant is easy built by VCC connected to R and serial with C to VSS.

The block diagram and electric
when PA0 input signal is 2.5V
option disabled. This block fur
reset.

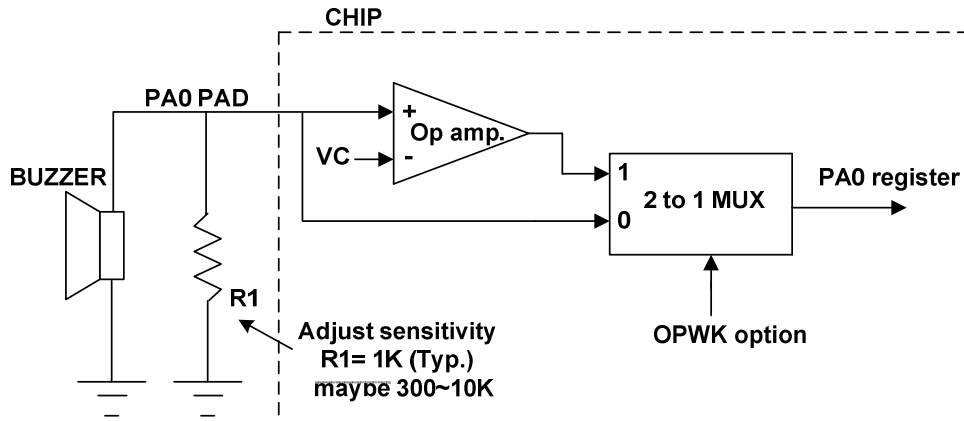
ffer shown below. It takes about 5uA
takes about 500uA current if RCWK
enabled by hardware after power on

Analog signal



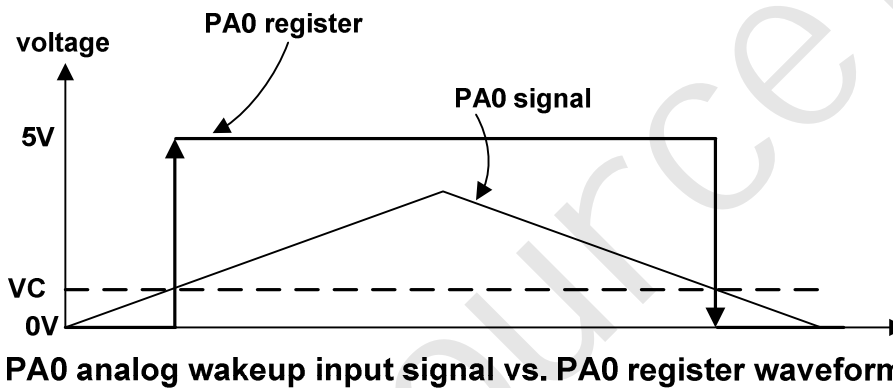


CST5080A OTP-type Speech IC



PA0 analog wakeup block diagram and buzzer trigger application circuit

Figure8. PA0 buzzer wake up structure



PA0 analog wakeup input signal vs. PA0 register waveform

Figure9. PA0 register waveform

5.13.2 Port PB (input/output)

The Port B is 4-bit bidirectional I/O port. Their directions can be defined by IOC_PB bit by bit.

The following table describe the SFRs associated with Port B.

Symbol	Addr	R/W type	Reset	D3	D2	D1	D0	Description
IOC_PB	05H	R/W	0000	IOCB3	IOCB2	IOCB1	IOCB0	"1" = output, "0" = input of related PB bit.
DATA_PB	06H	R/W	xxxx	DPB3	DPB2	DPB1	DPB0	Read from Port B input port and write to output port.

Table 15: SFRs of Ports PB

In output mode, the data can be written out to external pin, and reading this output port will read the data internal latch. Pull-down resistor will be disabled when output mode is selected.

In input mode, Port B data can be read from external pin, and they are attached with 1M/50K Ohm pull-down resistor or not according to the options.

In addition, each pin of Port B also can be accompanied with wake-up function according to the options.

In HALT mode, if some bits of Port B are accompanied with wake-up function, any rising edge occurred on that pin will wake-up system and turn on oscillator, and the program counter of MCU will jump to the address 0x0004. This device will start to execute the wake-up sub-routing.



CST5080A OTP-type Speech IC

5.13.3 Port PC (output) Selected by option.

The Port C is 4-bits output only port.

The following table describe the SFRs associated with Port C.

Symbol	Addr	R/W type	Reset	D3	D2	D1	D0	Description
DATA_PC	04H	R/W	0000	DPC3	DPC2	DPC1	DPC0	Port C is output port only. Write to Port C output port.

Table 16: SFR of Port PC

5.13.4 Port PE (input) Selected by option.

All 4-bits of the Port E are input ports only. They are accompanied with 1M/50K Ohm pull-down resistor or not according to the options.

The following table describe the SFRs associated with Port E.

Symbol	Addr	R/W type	Reset	D3	D2	D1	D0	Description
DATA_PE	0EH	R/W	xxxx	DPE3	DPE2	DPE1	DPE0	Port E defined as I/O port or input port depends on option PEIO. Read from Port E input port and write to output port.

Table 17: SFR of Port PE

5.13.5 Port PCE (input/output) Selected by option "PCEIO".

Whether all 4-bits of the Port E are input or output ports depends on IOC_PCE control register. They are accompanied with 1M/50K Ohm pull-down resistor or not according to the options if they are in the input mode.

The following table describe the SFRs associated with Port CE.

Symbol	Addr	R/W type	Reset	D3	D2	D1	D0	Description
IOC_PCE	01H	R/W	0000	IOCE3	IOCE2	IOCE1	IOCE0	Enable when option "PEIO" selected. "1" = output, "0" = input of related PE bit.
DATA_PCE	04H	R/W	0000	DPCE3	DPCE2	DPCE1	DPCE0	Port CE is output port only. Write to Port CE output port.

Table 18: SFR of Port PCE

There are three modes on Port PCE. They are single OP mode, two comparators mode and comparator & OP mode shown in table below.

Item	Port PCE Structure	Relative Options	Reference Figure
Mode 1	Single OP mode	OPEN	Figure 10
Mode 2	Two comparators mode	CMPEN1、CMPEN2、B1RZ、B3RZ	Figure 11
Mode 3	Comparator & OP mode	CMPEN1、OPEN、B1RZ	Figure 12

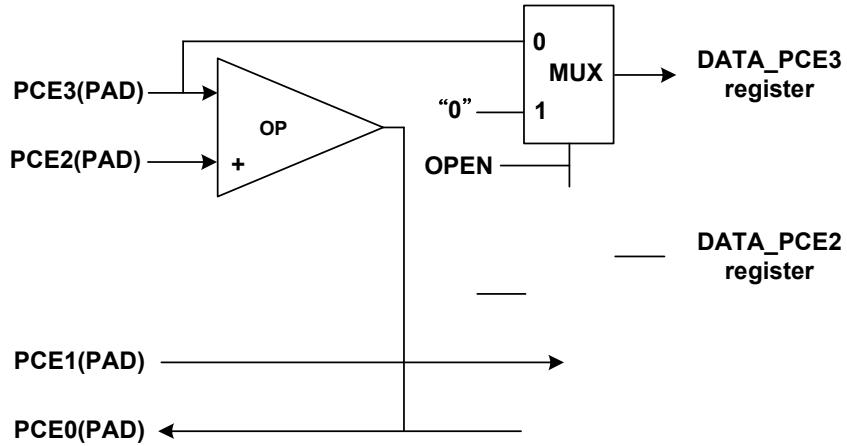
Table 19: Structure of PCE

These three modes can be enabled by option OPEN, CMPEN1 and CMPEN2. Option B1RZ is used for reading control DATA_PCE1. If B1RZ is enabled, DATA_PCE1 will read always 0. Otherwise, it will read the state of external Port PCE1. Another option B3RZ is the same function as B1RZ. Option B3RZ is used for reading control DATA_PCE3.

Mode1. Single OP mode

Port PCE provides one OP, if option OPEN is enabled. In this mode, the positive, negative input and output pin of OP is configured as below. In order to avoid interference between PCE1 and PCE2 pin, it's recommended PCE1 must be set as input port.

Notice: If option OPEN function enabled, ENGAIN function should be disable.





CST5080A OTP-type Speech IC

Option B1RZ is used for reading control DATA_PCE1. If B1RZ is enabled, DATA_PCE1 will read always 0. Otherwise, it will read the state of external Port PCE1. Another option B3RZ is the same function as B1RZ. Option B3RZ is used for reading control DATA_PCE3. The option B1RZ & B3RZ configuration as shown below.

Option CMPEN1 & B1RZ configuration

CMPEN1	CMPEN2 & OPEN	B1RZ	Reading DATA_PCE1~0
0	0	X	Port PCE is pure I/O port
1	0	0	Reading DATA_PCE1 register comes from the PCE1 external Port Reading DATA_PCE0 register comes from the output of comparator1
1	0	1	Reading DATA_PCE1 register is always 0 Reading DATA_PCE0 register comes from the output of comparator1

Table 20. Port PCE comparator1 configuration

Option CMPEN2 & B3RZ configuration

CMPEN2	CMPEN1 & OPEN	B3RZ	Reading DATA_PCE3~2
0	0	X	Port PCE is pure I/O port
1	0	0	Reading DATA_PCE3 register comes from the PCE3 external Port Reading DATA_PCE2 register comes from the output of comparator2
1	0	1	Reading DATA_PCE3 register is always 0 Reading DATA_PCE2 register comes from the output of comparator2

Table 21. Port PCE comparator2 configuration

Mode3. Comparator and OP mode

Port PCE provides comparator and OP mode if option CMPEN1 and OPEN are enabled. Option CMPEN2 must be disabled. In this mode, the comparator and OP is configured as below. It's suitable for small signal detect used on remote toy car applications.

Notice: If option OPEN function enabled, ENGAIN function should be disable.

Option OPEN, CMPEN1 & B1RZ configuration

OPEN	CMPEN1	CMPEN2	B1RZ	Reading DATA_PCE3~0
0	0	0	x	Port PCE is pure I/O port
1	1	0	0	Reading DATA_PCE2 or DATA_PCE3 register is always 0 Reading DATA_PCE1 register comes from the PE1 external Port Reading DATA_PCE0 register comes from the output of comparator1
1	1	0	1	Reading DATA_PCE2 or DATA_PCE3 register is always 0 Reading DATA_PCE1 register is always 0 Reading DATA_PCE0 register comes from the output of comparator1

Table 22. Port PCE option B1RZ configuration



CST5080A OTP-type Speech IC

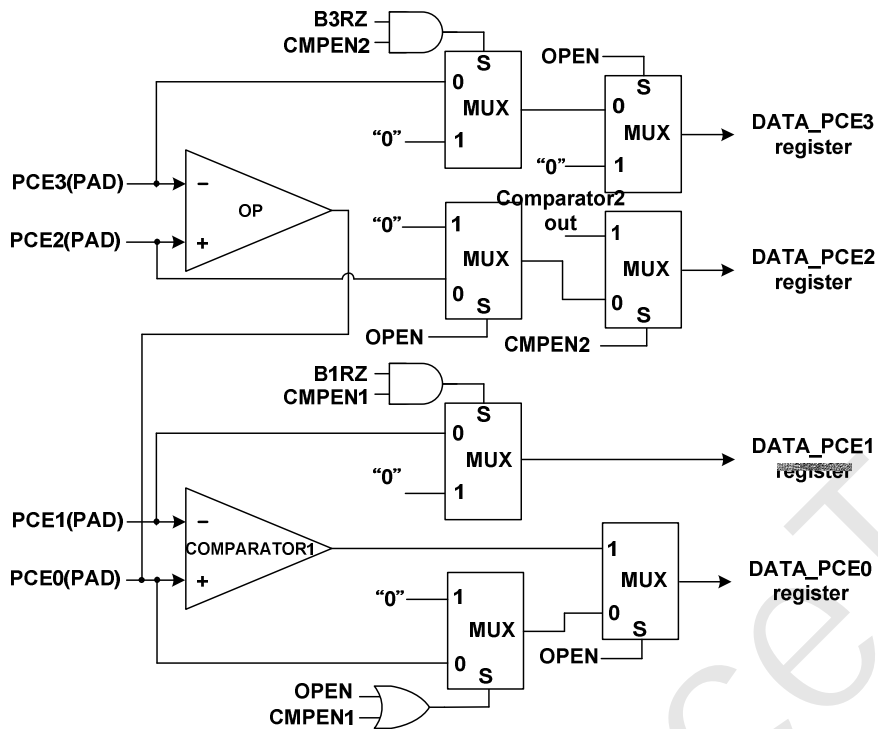
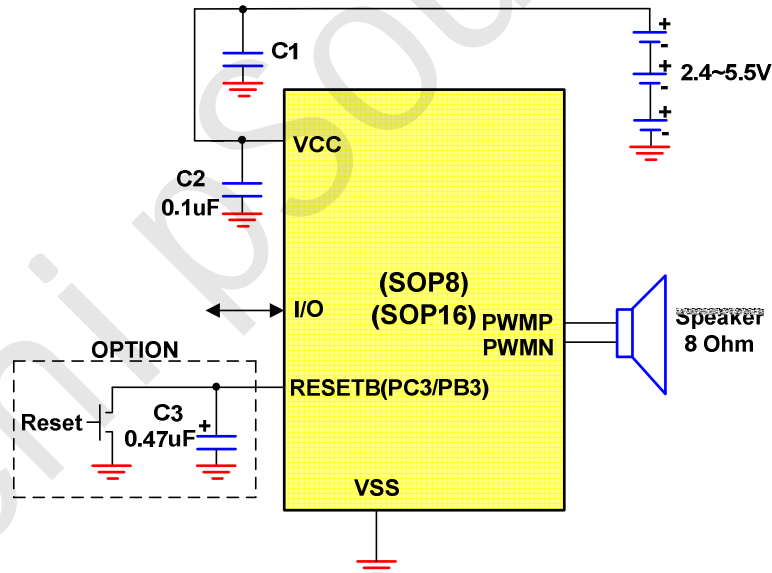


Figure 12. Port PCE mode 3 block diagram

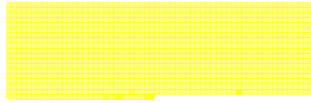
6. CST5080A The Application Circuit



Note : Substrate must be connected to VSS.

Figure 13. PWM Applications circuit

DAC Selected by option





CST5080A OTP-type Speech IC

OPEN	OPA @ PCE3(in-),PCE2(in+),PCE0(out)
PD220K	Change 50K Ohm pull-down resistor to 220K Ohm
CMP #1	Comparator #1 control
CMP #2	Comparator #2 control
PWM12S	PWM 12 bit select
PWM10S	PWM 10/8 bit select
LOPENC	Output weak low for PC3~PC0
OTPLOCK	Security control
F38K	PA3 38KHz output
BIWK	Bi-directional wake up
OPTADJ	OSC IADJ select
PCEIO	Port CE I/O mode control
HDEN	Driving capacity of output port control
PCESEL	Port CE as PC/PE select
B3RZ	PE3 mode select when CMP enable
B1RZ	PE1 mode select when CMP enable

8. CST5080A The Revision History

Version	Description	Page	Date
1.0	Established		2021-01-04
1.1	Cancel CST5066		2021.04.06

Table 23: Revision History