TRSP(M)5018A OTP-type Speech IC

1. TRSP(M)5018A General Descriptions

TRSP(M)5018A series are 4-bits micro-controller which could play 4 channel melody or 4 channel ADPCM with PWM direct drive circuit. PWM resolution is 8/10/12 bits. They includes a low cost, high performance CMOS micro-processor. The clock frequency of this up is typically 8.192 (±3%) MHz. This chip operates over a wide voltage range of 2.0V~5.5V. It contains program ROM (PROM) and data ROM (DROM) inside. The maximum program ROM is 4K words and maximum data ROM size is 56K byte. The maximum working SRAM is (64+2) nibbles. It is provided with total 4 software programmable I/O Ports.

2. TRSP(M)5018A Features

- Operating voltage: **2.0V to 5.5V**
- MCU Operation frequency: **8.192MHz**
- Memory Size
  - Program ROM size: **4K*12-bits OTP type**
  - Data ROM size: **56K*8-bits OTP type**
  - SRAM size: **64*4 bits**
  - User register: **2*4 bits**
- Wakeup function for power-down mode:
  - HALT mode wakeup source: Port A can wake-up from HALT mode to NORMAL mode and executing wake-up sub-routine program.
- 4 input/output pins: Port A can be defined as input or output port bit by bit.
- Three reset condition:
  - Low voltage reset. (LVR = 2.0V)
  - Power on reset.
  - Watch dog timer overflow.
- One internal interrupt sources:
  - PWM interrupt.
- WDT
  - Watch dog timer, can enabled/disabled by option.
  - WDT period is 256*256*16/Fsys. (WDT period is 0.13 sec for system clock=8.192MHz)
- Audio output:
  - Support PWM or DAC mode by option.
  - Support 8/10/12 bits.
- Support option set for pull down resistor 1M, 50K or 220K Ohm, low voltage reset…etc.
- Oscillator fuse option **±3%, temperature & voltage compensation.**
- Support **security option (1 bit)** for read inhibition.
- Support 16-levels LVD function.

3. TRSP(M)5018A Packaging and Pads Information

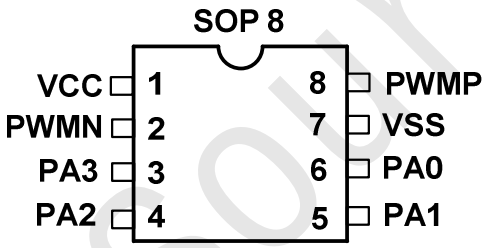
3.1 Pads

VCC	P	High	Power input of I/O port.
VSS	P	Low	Ground input except PWM block power. It could be double bonded with VPS pad.
VPD	P	High	PWM block power input in normal operation.
VPS	P	Low	The ground pad of PWM block. It could be double bonded with VSS pad.
PA3~PA0	I/O	zzzz	Port A is a programmable input/output port.
PWMP	O	Low	Audio output PWM(+).
PWMN	O	Low	Audio output PWM(-).

Table 1: Pad Description

3.2 Package

TRSP(M)5018A provides SOP8



4. TRSP(M)5018A ELECTRICAL CHARACTERISTICS

4.1 Absolute Maximum Ratings

DC Supply Voltage	Vcc	-0.5 to 6.0	V
Input Voltage	Vin	-0.5 to Vcc+0.5	V
Operating Temperature Range	Ta	0 to +75	℃
Storage Temperature Range	Tstg	-25 to +85	℃

Table 2: Absolute Maximum Ratings

4.2 AC Characteristics

VCC=3.0V, Ta=25℃ unless otherwise noted.

Operating Frequency(RC Oscillator)	Fsys	7.946MHz	8.192 MHz	8.43MHz
RC reset time-constant	Trrc	-	10 us	-
Data ROM data ready time	Tdrr	-	-	2/Fsys

Table 3: AC Characteristics

4.3 DC Characteristics

VCC=3.0V, Ta=25℃ unless otherwise noted.

Parameters	Symbol	Minimum	Typical	Maximum	Condition
Power supply range	Vcc	2.0 V	-	5.5 V	
OTP Programming Power	Vpp	9.5 V	10 V	10.5 V	VCC = 4.8V
Supply current	Iop		5mA		System clock 8.192MHz PWM disabled
Stand-by Current	I_{STBY}		3uA		VCC=5.0V, MCU halt System clock off
Input high voltage	Vih		0.55 VCC		
Input low voltage	Vil		0.55 VCC		
Input leakage current	Ilk		0.1 uA		
Output high voltage	Voh	0.95 VCC			no load
Output low voltage	Vol			0.05 V	no load
Output high current in high source capacity mode	Ioh0		20mA		Vout=2.0 all ports High source capacity
Output low current in high sink capacity mode	Iol0		20mA		Vout=1.0 all ports High sink capacity
Output high current in normal source capacity mode	Ioh1		4mA		Vout=2.0 all ports Normal source capacity
PWM output load		-		8 ohm	Speaker impedance
Pull-down resistance #1	Rpd1	-	50K Ohm	-	PA pins with pull-down Vin=3.0V
Pull-down resistance #2	Rpd2		220K Ohm		PA pins with pull-down Vin=3.0V
Pull-down resistance #3	Rpd3		1M Ohm		PA pins with pull-down Vin=3.0V
Threshold voltage of low voltage reset circuit	Vlvr		2.0V		Low voltage reset circuit can't be disabled

Table 4: DC Characteristics

5. TRSP(M)5018A FUNCTIONAL DESCRIPTION

This chapter describes the function of MCU.

5.1 Program ROM (PROM)

The PROM is an OTP (One Time Programmable) type memory. The **PROM is 4K*12-bits (0000H ~ 1FFFH)** which stores execution program. The last 256 location of effective PROM is reserved area, the user shall not use this area in any case. Assembler shall check user program on this limit. Hardware does not need to check this restriction.

In order to reserved unused area of PROM. These regions maybe use in the future. There is one option "OTPREV" for this purpose. If all unused area of PROM wanted to fill with "0xFFF", the option "OTPREV" on IDE tool must be enabled.(h)1.4(e)1.48Oved unthevhhese7915 5.763.9(R)-1.3(E)3se7915 .9(p)1.b05(-)-41i879565.763.9(

PROM address	Function description
0x000 ~ 0x001	Reset
0x004 ~ 0x005	Wake-up
0x008 ~ 0x009	Interrupt
0x00A ~ 0xEFF	User code
0xF00 ~ 0xFFF	Reserve area

Table 3: Memory Map of PROM

5.2 Data ROM (DROM)

The DROM is an OTP (One Time Programmable) type memory. The maximum **DROM is 56K*8-bits** which stores the 8-bits wide data for ADPCM or melody data …etc. The last 64 location is a reserved area. The user shall not use this area in any case. Assembler shall check user data ROM on this limit. Hardware does not need to check this restriction.

DROM address (DMA)	Function description
0x0000 ~ 0x00FF	User area
0x0100 ~ 0x01FF	User area
0x0200 ~ 0x02FF	User area
…	…
0xDFB0 ~ 0xDFBF	User area (Max. size of TRSP(M)5018A)
0xDFC0 ~ 0xDFFF	System area, last 64 location(don't use it)

Table 4: Memory Map of DROM

DROM is addressed by four registers DMA3, DMA2, DMA1 and DMA0. After these registers are specified by software, the data need enough delay time, Tdrr in the table of "AC Characteristics". After this delay time, the data can be read from data register (DMDL & DMDH).

Ex:

```
LD      (DMA0), A
…
LD      (DMA3), A       ; Set DMA0~3
LD      A, (DMDL)       ; Read low nibble data from DROM, address as DMA3~0.
LD      A, (DMDH)       ; Read high nibble data from DROM, address as DMA3~0.
```

Symbol	Addr	R/W type	Reset	D3	D2	D1	D0	Description
DMA0	18H	R/W	xxxx	DMA0.3	DMA0.2	DMA0.1	DMA0.0	DMA0~3, four register built a 16-bits addressing space for read DROM 8-bits data. DMA0 is lowest nibble, DMA3 is highest nibble of DROM address.
DMA1	19H	R/W	xxxx	DMA1.3	DMA1.2	DMA1.1	DMA1.0	
DMA2	1AH	R/W	xxxx	DMA2.3	DMA2.2	DMA2.1	DMA2.0	
DMA3	1BH	R/W	xxxx	DMA3.3	DMA3.2	DMA3.1	DMA3.0	
DMDL	1CH	R/W	xxxx	DMDL.3	DMDL.2	DMDL.1	DMDL.0	Low nibble of DROM data read from this address.
DMDH	1DH	R/W	xxxx	DMDH.3	DMDH.2	DMDH.1	DMDH.0	High nibble of DROM data read from this address. Write this register means reset watch dog timer if this timer is enabled by option.

Table 5: SFRs about DROM

<table>
<tr><td>AUD_DH</td><td>0BH</td><td>W</td><td>xxxx</td><td>AUD_DH3</td><td>AUD_DH2</td><td>AUD_DH1</td><td>AUD_DH0</td><td>AUD_DH[3:0]:
The high nibble of 8 bits PWM.
The bit9~6 of 10 bits PWM.
The bit11~8 of 12 bits PWM.
Note: AUD_DH3 is sign bit, “0” means positive.</td></tr>
<tr><td>Reserved</td><td>0CH~
0EH</td><td>-</td><td>xxxx</td><td>-</td><td>-</td><td>-</td><td>-</td><td>Reserved</td></tr>
<tr><td>USER2</td><td>0FH</td><td>R/W</td><td>xxxx</td><td>USER2.3</td><td>USER2.2</td><td>USER2.1</td><td>USER2.0</td><td>General purpose user register.</td></tr>
<tr><td>IADJ</td><td>10H</td><td>R/W</td><td>0000</td><td>CMPSEL1</td><td>CMPSEL0</td><td>ADJ1</td><td>ADJ0</td><td>CMPSEL[1:0]:
Enable option PCEIO, ENOP, ENCMP1, and set ENGAIN=1, Select Gain in record mode.
<table>
<tr><th>CMPSEL[1:0]</th><th>GAIN</th></tr>
<tr><td>00</td><td>50</td></tr>
<tr><td>01</td><td>100</td></tr>
<tr><td>10</td><td>150</td></tr>
<tr><td>11</td><td>200</td></tr>
</table>
ADJ[1:0]:
Adjust the frequency, when enable option OTPADJ.
<table>
<tr><th>ADJ[1:0]</th><th>Frequency %</th></tr>
<tr><td>00</td><td>-4%</td></tr>
<tr><td>01</td><td>-2%</td></tr>
<tr><td>10</td><td>2%</td></tr>
<tr><td>11</td><td>4%</td></tr>
</table></td></tr>
<tr><td>CNTI</td><td>11H</td><td>R/W</td><td>0000</td><td>ENGAIN</td><td>-</td><td>S2S</td><td>-</td><td>ENGAIN:
1: Open Built-in gain in record mode.
0: Close Built-in gain in record mode.
S2S: PWM input Data format
1: 2's format
0: sign
Notice: If ENGAIN enabled, option OPEN function should be disable.</td></tr>
<tr><td>PWMWK</td><td>12H</td><td>R/W</td><td>0000</td><td>PWMWKFG</td><td>CLAPSEL1</td><td>CLAPSEL0</td><td>PWMWKEN</td><td>PWMWKFG：
When wakeup source form Speaker, it will be set by hardware, it could be clear by software.
PWMWKEN: Wakeup by speaker.
1: Enable PWM wakeup function.
0: Disable PWM wakeup function.
CLAPSEL[1:0]: Sensitivity of speaker wakeup.
<table>
<tr><th>CLAPSEL[1:0]</th><th>Sensitivity</th></tr>
<tr><td>00</td><td>Level 1 (low)</td></tr>
<tr><td>01</td><td>Level 2</td></tr>
<tr><td>10</td><td>Level 3</td></tr>
<tr><td>11</td><td>Level 4 (High)</td></tr>
</table></td></tr>
<tr><td>LVD_CTRL</td><td>13H</td><td>R/W</td><td>0000</td><td>-</td><td>-</td><td>LVD_FLAG
(R)</td><td>LVDEN</td><td>LVD_FLAG: (Read only)
The flag of LVD, '1'=LVD sensing.
LVDEN:
'1'=Enable LVD function,
'0'=Disable LVD function.</td></tr>
<tr><td>LVDS</td><td>14H</td><td>R/W</td><td>0000</td><td>LVDS3</td><td>LVDS2</td><td>LVDS1</td><td>LVDS0</td><td>LVDS[3:0]: LVD level selected,
1111=3.8V, 1110=3.7V, 1101=3.6V, 1100=3.4V,
1011=3.3V, 1010=3.2V, 1001=3.1V, 1000=3.0V,
0111=2.9V, 0110=2.8V, 0101=2.7V, 0100=2.5V,
0011=2.4V, 0010=2.3V, 0001=2.2V, 0000=2.1V.</td></tr>
<tr><td>Reserved</td><td>15H~
17H</td><td>-</td><td>xxxx</td><td>-</td><td>-</td><td>-</td><td>-</td><td>Reserved</td></tr>
<tr><td>DMA0</td><td>18H</td><td>R/W</td><td>xxxx</td><td>DMA0.3</td><td>DMA0.2</td><td>DMA0.1</td><td>DMA0.0</td><td rowspan="2">DMA0~3, four register built a 16-bits addressing space for read DROM 8-bits data, DMA0 is</td></tr>
<tr><td>DMA1</td><td>19H</td><td>R/W</td><td>xxxx</td><td>DMA1.3</td><td>DMA1.2</td><td>DMA1.1</td><td>DMA1.0</td></tr>
</table>

DMA2	1AH	R/W	xxxx	DMA2.3	DMA2.2	DMA2.1	DMA2.0	lowest nibble, DMA3 is highest nibble of DROM address.
DMA3	1BH	R/W	xxxx	DMA3.3	DMA3.2	DMA3.1	DMA3.0	
DMDL	1CH	R/W	xxxx	DMDL.3	DMDL.2	DMDL.1	DMDL.0	Low nibble of DROM data read from this address.
DMDH	1DH	R/W	xxxx	DMDH.3	DMDH.2	DMDH.1	DMDH.0	High nibble of DROM data read from this address. Writing this register means reset watch dog timer if this timer is enabled by option.
Reserved	1EH~ 1FH	-	xxxx	-	-	-	-	Reserved

Table 7: All of the Special Function Registers

5.4 Interrupt Vector Address

Vector	Address
RESET	00H
WAKEUP	04H

2. HALT Mode: In HALT mode, the MCU clock stops, users can't change the operation mode when in halt mode. It will go back to NORMAL mode (Program counter=0x004) when I/O wakeup or reset occurred. Please refer to the section of" Halt Mode & Wake up" for the detailed HALT mode description.

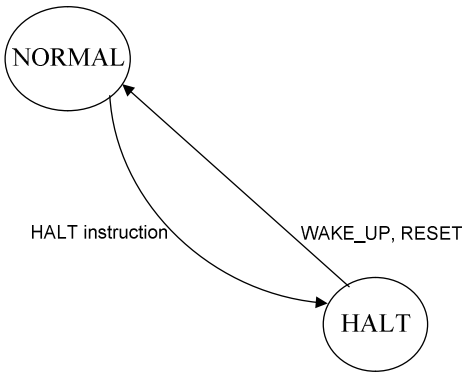


Figure 2: Clock Operation Mode

5.7 Halt Mode & Wake up

The MCU is changed into HALT mode (program counter and system clock stop) when HALT instruction executed. It provides a power saving mode for those applications requiring a very low stand-by current. The PA[3:0] are supporting the wake-up function when rising edge occurred.

The program counter will be 0x004 when HALT instruction executed immediately, then program counter will go to next address after 64 stable clock(system clock) when wake up condition occurred. Reset signal will release HALT state and execute reset procedure because reset is first priority when in HALT mode, so program counter will from 0x004 to 0x000, program counter goes to next address after 64 stable clock cycles. Furthermore, the SRAM will keep their previous data without changing in this mode.

5.8 Watch Dog Timer Reset (WDT)

The **Watch Dog Timer (WDT)** is used to reset whole chip when detect unexpected execution sequence caused by accident condition, avoiding dead lock of MCU program. WDT will be reset when wake-up from halt, after reset or software clears it. The watch dog timer is a simple counter. It has a fixed length of **256*256*16/system-clock (ex: 0.13 sec for 8.192MHz system clock)** after the clearance of watch dog.

Software must run a "clear watch dog timer" (write to DMDH) instruction before this timer time out when WDT enabled. It will generate a reset signal to reset whole system when WDT over flow. Assembler will check user program about the "reset watch dog" instructions. If more than one "reset watch dog" is found in program, assembler will generate a warning (program code will still be generated). "HALT" instruction will reset watch dog timer. The reset watch dog timer sequence is strongly recommended as:

```
WATCHDOG:
        LD      (1DH), A
```

5.9 Low Voltage Detect (LVD)

The low voltage detect (LVD) function is used to detect whole chip power supply VCC. TRSP(M)5018A support 16-level LVDS[3:0] to selected detect voltage level, the detected voltage range is from 3.8V to 2.1V.

There have one control register LVDEN used to enable/disable the low voltage detect function. The flag signal LVD_FLAG is used to check the power supply VCC upper or under than low voltage detect level, when VCC upper than LVD level, the flag LVD_FLAG value is low; otherwise, the flag LVD_FALG value is high when VCC under than VCC.

Symbol	Addr	R/W type	Reset	D3	D2	D1	D0	Description
LVD_CTRL	13H	R/W	0000	-	-	**LVD_FLAG (R)**	**LVDEN**	**LVD_FLAG: (Read only)** The flag of LVD, '1'=LVD sensing. **LVDEN:** '1'=Enable LVD function, '0'=Disable LVD function.
LVDS	14H	R/W	0000	**LVDS3**	**LVDS2**	**LVDS1**	**LVDS0**	**LVDS[3:0]:** LVD level selected, 1111=3.8V, 1110=3.7V, 1101=3.6V, 1100=3.4V, 1011=3.3V, 1010=3.2V, 1001=3.1V, 1000=3.0V, 0111=2.9V, 0110=2.8V, 0101=2.7V, 0100=2.5V, 0011=2.4V, 0010=2.3V, 0001=2.2V, 0000=2.1V.

5.10 8/10/12 Bits PWM/DAC

There are three optional PWM/DAC output resolutions. One is 8-bits output, the sec. is 10-bits output, and the other is 12-bits output. The highest of input data is signed bit: '0' represents positive, '1' represents negative.

TRSP(M)5018A supports audio output with PWM and DAC two modes. These two modes can be selected by "DACEN" option. If use DAC output mode, option "DACEN" must be enabled. Otherwise, PWM mode is enabled. All PWM registers will be exchanged for DAC mode if "DACEN" option is enabled.

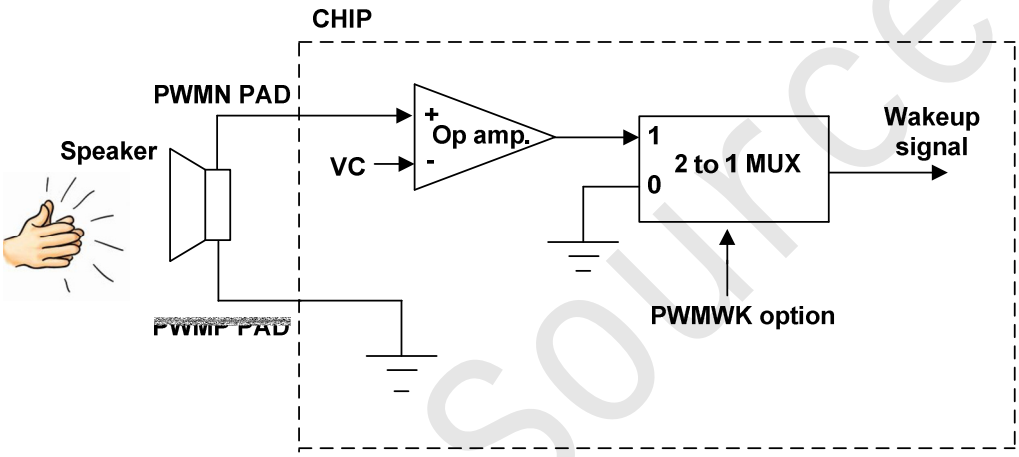
Symbol	Addr	R/W type	Reset	D3	D2	D1	D0	Description
STATUS	00H	R/W	00xx	reserved	**PWFG**	CF	ZF	Status Register **PWFG:** PWM interrupt flag. CF: Carry flag. ZF: Zero flag.
AUD_DLL	08H	W	xxxx	**AUD_DLL3**	**AUD_DLL2**	**AUD_DLL1**	**AUD_DLL0**	**AUD_DLL[3:2]:** The bit1~0 of 10-bits PWM, combine with AUD_DL[3:0], AUD_DH[3:0] to built 10-bits PWM if option PWM10 is 1 and PWM12 is 0. **AUD_DLL[3:0]:** The bit3~0 of 12-bits PWM, combine with AUD_DL[3:0], AUD_DH[3:0] to built 12-bits PWM if option PWM12 is 1.
PWM_CTRL	09H	R/W	--x0	reserved	reserved	**ENINT**	**ENPWM**	**ENPWM:** "1" Enable PWM, "0" Disable PWM. **ENINT:** Enable global interrupt.
AUD_DL	0AH	W	xxxx	**AUD_DL3**	**AUD_DL2**	**AUD_DL1**	**AUD_DL0**	**AUD_DL[3:0]:** The low nibble of 8-bits PWM. The bit5~2 of 10-bits PWM. The bit7~4 of 12-bits PWM.
AUD_DH	0BH	W	xxxx	**AUD_DH3**	**AUD_DH2**	**AUD_DH1**	**AUD_DH0**	**AUD_DH[3:0]:** The high nibble of 8 bits PWM. The bit9~6 of 10 bits PWM. The bit11~8 of 12 bits PWM. Note: AUD_DH3 is sign bit, "0" means positive.

Table 10: SFRs about the operation of PWM

Symbol	Addr	R/W type	Reset	D3	D2	D1	D0	Description
PWMWK	12H	R/W	0000	PWMWKFG	CLAPSEL1	CLAPSEL0	PWMWKEN	**PWMWKFG**： When wakeup source form Speaker, it will be set by hardware, it could be clear by software. **PWMWKEN:** Wakeup by speaker. 1: Enable PWM wakeup function. 0: Disable PWM wakeup function. **CLAPSEL[1:0]:** Sensitivity of speaker wakeup.

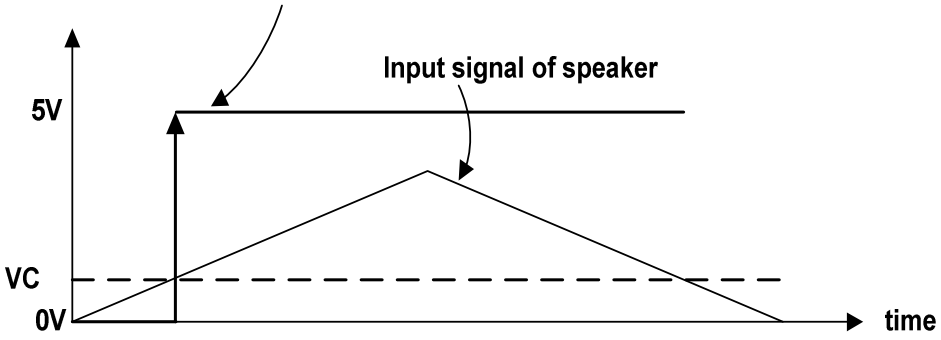
CLAPSEL[1:0]	Sensitivity
00	Level 1 (low)
01	Level 2
10	Level 3
11	Level 4 (High)

Table 13: SFRs about the operation of speaker wakeup function



Wakeup control block diagram and speaker trigger application circuit

Figure 3: Speaker wakeup structure



Input signal of speaker vs

5.13 I/O Ports

There is one I/O port PA3~PA0, whose input/output direction are defined by IOC_PA. The wake-up functions of PA3~PA0 are enabled or disabled by option. All I/O ports provides rising or falling edge wake up function. This double edge wake up function can be enabled by "BIWK" option. Their 1M/50K Ohm pull down resistors are optional.

In order to achieve touch function, TRSP(M)5018A support 220K Ohm pull down resistors. These resistors can be enabled by using 50K Ohm pull down resistor registers after "PD220K" is enabled. The 220K Ohm resistance value is almost fixed value when VCC change from 2.0V to 5.5V.

5.13.1 Port PA (input/output)

The Port A is 4-bits bidirectional I/O port. Their directions can be defined by IOC_PA bit by bit.
The following table describe the SFRs associated with Port A.

Symbol	Addr	R/W type	Reset	D3	D2	D1	D0	Description
IOC_PA	02H	R/W	0000	**IOCA3**	**IOCA2**	**IOCA1**	**IOCA0**	**"1" = output, "0" = input of related PA bit.**
DATA_PA	03H	R/W	xxxx	**DPA3**	**DPA2**	**DPA1**	**DPA0**	**Read from Port A input port and write to output port.**

Table 14: SFRs of Ports PA

In output mode, the data can be written out to external pin, and reading this output port will read the data internal latch. Pull-down resistor will be disabled when output mode is selected.
In input mode, Port A data can be read from external pin, and they are attached with 1M/50K Ohm pull-down resistor or not according to the options.

In addition, each pin of Port A also can be accompanied with wake-up function according to the options. In HALT mode, if some bits of Port A are accompanied with wake-up function, any rising edge occurred on that pin will wake up system and turn on oscillator, and the program counter of MCU will jump to the address 0x004. This device will start to execute the wake-up sub-routing.

PA3 is provided with 38KHz modulator
I/O port PA3 built-in a 38KHz modulator combined with register DATA_PA bit-3, this function is enabled by **"F38K" option**. If F38K option is enabled, I/O port PA3 will output 38KHz clock signal when PA3 is configured as output port and DATA_PA bit-3 = 1. PA3 output low when PA3 is configured as output port and DATA_PA bit-3 = 0.
Notice: The PA3 output pad will be forced to low state automatically by hardware control when in halt mode for avoid external IR LED destroyed. Besides, the F38K option disabled, PA3 is a normal I/O port.

PA0 is provided with an analog input (Schmitt) for wake-up control
PA0 supports an analog input buffer with Schmitt circuit, it is enabled by **"RCWK" option** and supports low power consumption in halt mode, if PA0 analog signal keep about 0.5*VCC, so this function is suitable for recycle wakeup MCU by external RC time constant, external RC time constant is easy built by VCC connected to R and serial with C to VSS.
The block diagram and electrical characteristic of PA0 analog input buffer shown below. It takes about 5uA when PA0 input signal is 2.5v @VCC=5V in halt mode, otherwise, it takes about 500uA current if RCWK option disabled. This block function is enabled when RCWK option enabled by hardware after power on reset.

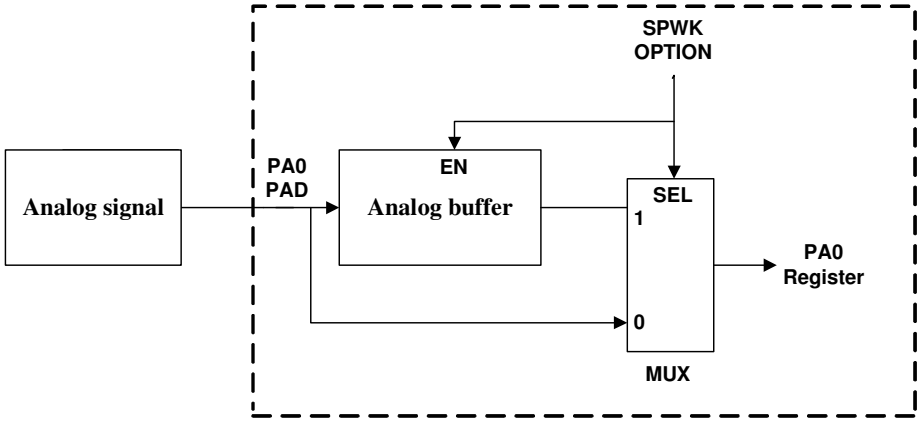


Figure 6. PA0 analog input structure

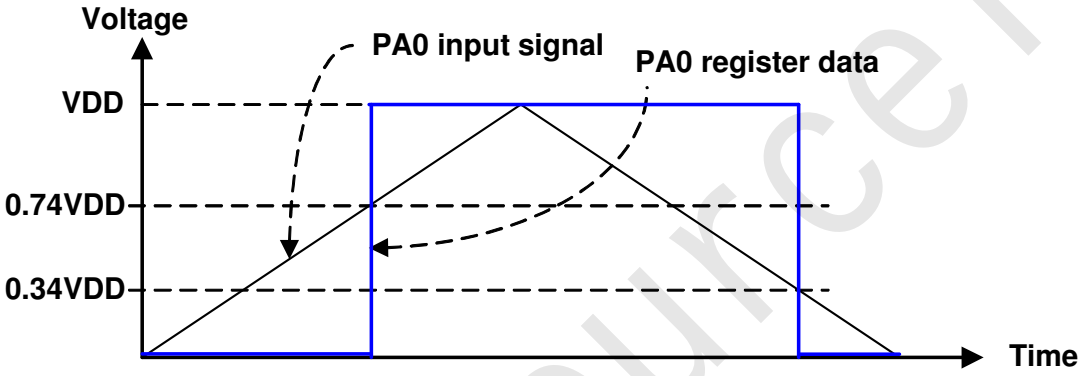


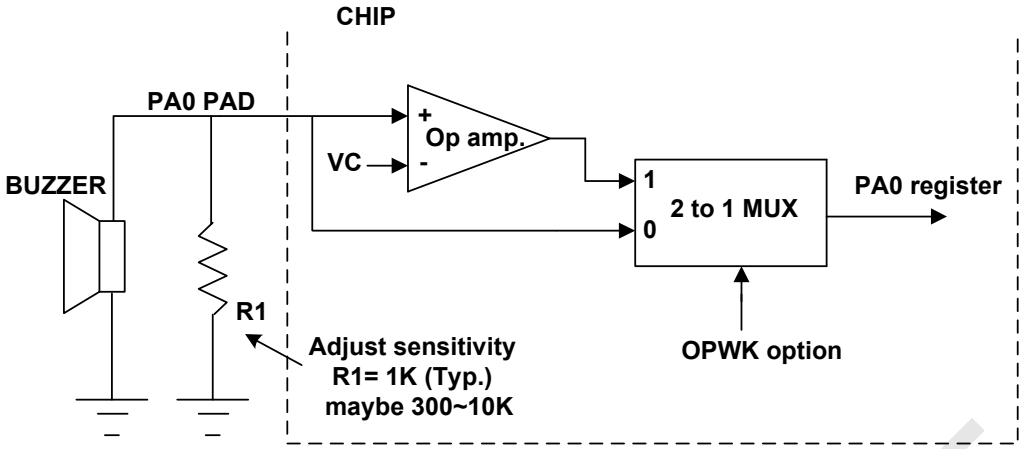
Figure 7. PA0 input signal and PA0 register data

PA0 is provided with an analog input (OP Amp.) for wake-up control

It built-in an OP amplifier for wake-up trigger, the pull down 1M and 50K Ohm resistor will be disabled by hardware circuit when **"BZWK" option** is enabled automatically, PA0 always keep at DC level (bias voltage Vbias) for signal amplify, and Vbias is about 0.8V~1.0V. (Wake-up by analog signal amplifier function is enabled by mask option **"BZWK**")

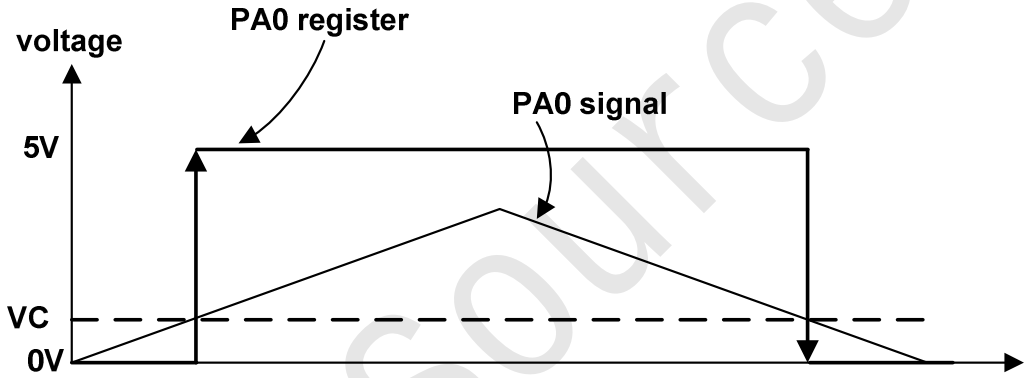
This block function is enabled when BZWK option is enabled by hardware after power on reset.

Notice: Buzzer function, please reference application note "AN-0068_V1.0" on TRITAN web site.



PA0 analog wakeup block diagram and buzzer trigger application circuit

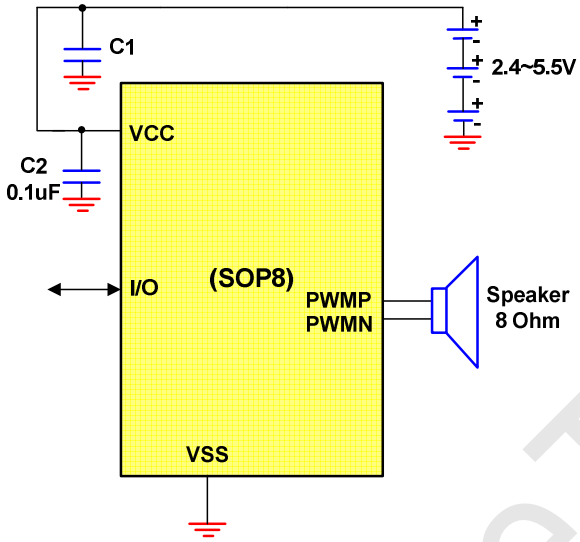
Figure 8. PA0 buzzer wake up structure



PA0 analog wakeup input signal vs. PA0 register waveform

Figure 9. PA0 register waveform

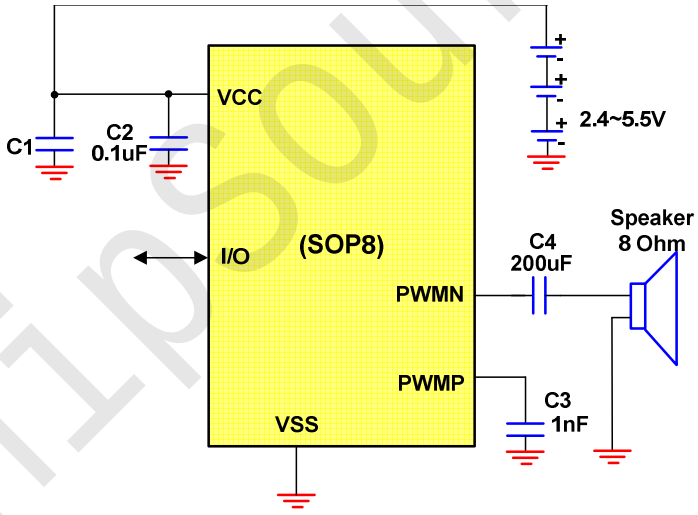
6. TRSP(M)5018A The Application Circuit



Note : Substrate must be connected to VSS.

Figure 10. PWM Applications circuit

DAC Selected by option



Note : Substrate must be connected to VSS.

Figure 11. DAC Applications circuit

Notice:

1. Regarding recording or remote car applications, please reference application note on TRITAN web site.
2. C1 : 47 uF ~ 100 uF(depends on applications), C2：0.1 uF
3. DAC Applications circuit not support PWM wakeup function.
4. DAC Applications, please reference application note on TRITAN web site.

7. TRSP(M)5018A Option Registers table

Option Name	Function Description
BZWK	PA0 buzzer trigger wakeup
RCWK	PA0 RC wakeup
PWM64K	PWM int. freq. select
DACEN	DAC function control
WAKEBA	Wake-up enable for PA3~PA0 respectively
PD50KPA	50K Ohm pull down resistor for PA3~PA0 respectively.
PD1MPA	1M Ohm pull down resistor for PA3~PA0 respectively.
WDGENB	Watch dog timer
HALTENB	HALT mode control
PD220K	Change 50K Ohm pull-down resistor to 220K Ohm
PWM12S	PWM 12 bit select
PWM10S	PWM 10/8 bit select
OTPLOCK	Security control
F38K	PA3 38KHz output
BIWK	Bi-directional wake up
OPTADJ	OSC IADJ select
HDEN	Driving capacity of output port control

8. TRSP(M)5018A The Revision History

Version	Description	Page	Date
1.0	Established		2021-01-04

Table 15: Revision History