TRSP5006A OTP-type Speech IC

1. TRSP5006A General Descriptions

TRSP5006A series are 4-bits micro-controller which could play 4 channel melody or 4 channel ADPCM with PWM direct drive circuit. PWM resolution is 8/10/12 bits. They includes a low cost, high performance CMOS micro-processor. The clock frequency of this up is typically 8.192 (±3%) MHz. This chip operates over a wide voltage range of 2.0V~5.5V. It contains program ROM (PROM) and data ROM (DROM) inside. The maximum program ROM is 4K words and maximum data ROM size is 33K byte. The maximum working SRAM is (64+2) nibbles. It is provided with total 4 software programmable I/O Ports.

2. TRSP5006A Features

- Operating voltage: **2.0V to 5.5V**
- MCU Operation frequency: **8.192MHz**
- Memory Size
  - Program ROM size: **4K*12-bits OTP type**
  - Data ROM size: **18K*8-bits OTP type**
  - SRAM size: **64*4 bits**
  - User register: **2*4 bits**
- Wakeup function for power-down mode:
  - HALT mode wakeup source: Port A can wake-up from HALT mode to NORMAL mode and executing wake-up sub-routine program.
- 4 input/output pins: Port A can be defined as input or output port bit by bit.
- Three reset condition:
  - Low voltage reset. (LVR = 2.0V)
  - Power on reset.
  - Watch dog timer overflow.
- One internal interrupt sources:
  - PWM interrupt.
- WDT
  - Watch dog timer, can enabled/disabled by option.
  - WDT period is 256*256*16/Fsys. (WDT period is 0.13 sec for system clock=8.192MHz)
- Audio output:
  - Support PWM or DAC mode by option.
  - Support 8/10/12 bits.
- Support option set for pull down resistor 1M, 50K or 220K Ohm, low voltage reset…etc.
- Oscillator fuse option **±3%, temperature & voltage compensation.**
- Support **security option (1 bit)** for read inhibition.
- Support 16-levels LVD function.

3. TRSP5006A Packaging and Pads Information

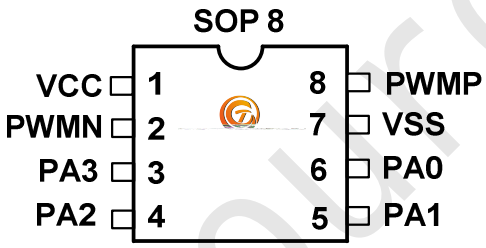
3.1 Pads

PAD Name	Type	State After Reset	Description
Reset, Power Input			
VCC	P	High	Power input of I/O port.
VSS	P	Low	Ground input except PWM block power. It could be double bonded with VPS pad.
VPD	P	High	PWM block power input in normal operation.
VPS	P	Low	The ground pad of PWM block. It could be double bonded with VSS pad.
General I/O ports			
PA3~PA0	I/O	zzzz	Port A is a programmable input/output port.
Audio output pads			
PWMP	O	Low	Audio output PWM(+).
PWMN	O	Low	Audio output PWM(-).

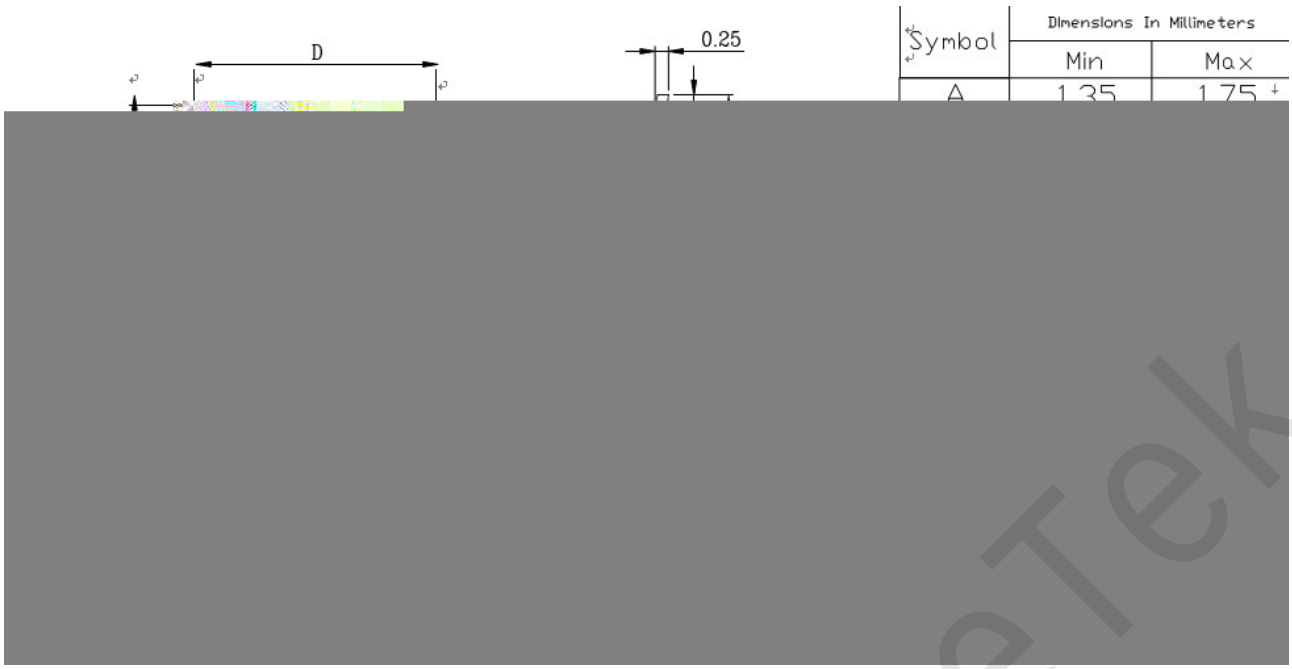
Table 1: Pad Description

3.2 Package

TRSP5006A **provides SOP8**



3.2.1 SOP8



3.3 Block Diagram

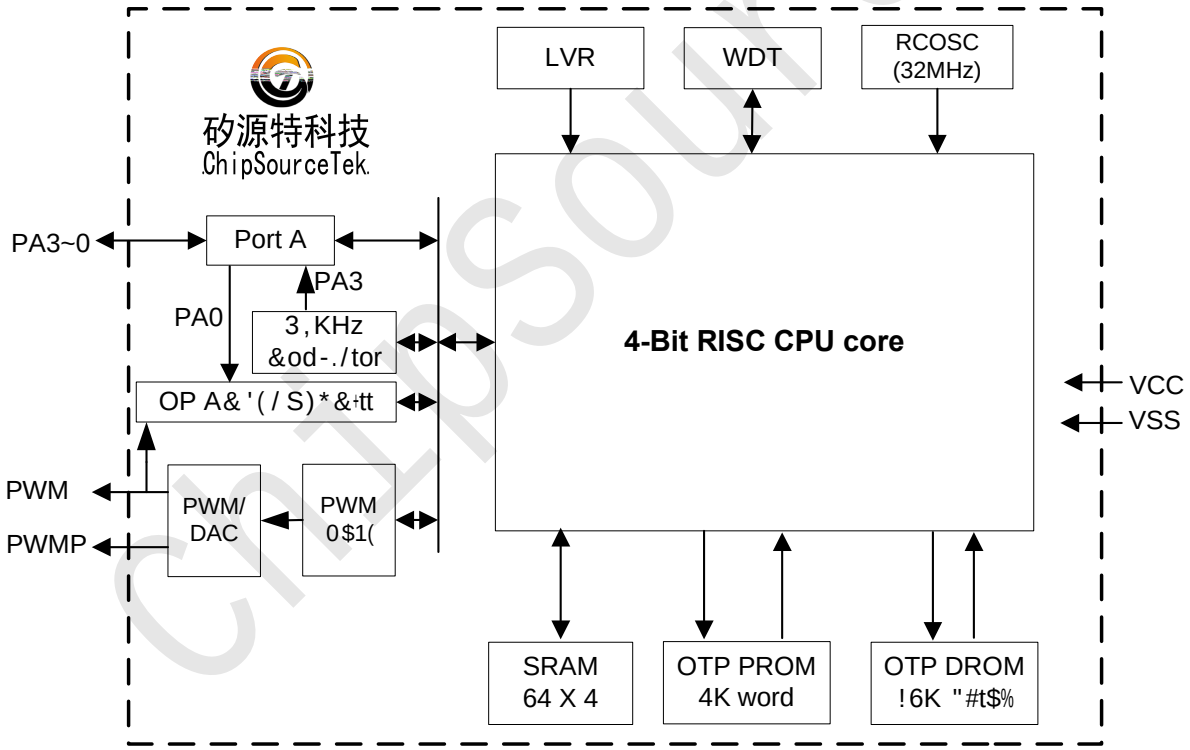


Figure 1. Block diagram

4. TRSP5006A ELECTRICAL CHARACTERISTICS

4.1 Absolute Maximum Ratings

Parameters	Symbol	Value	Unit
DC Supply Voltage	Vcc	-0.5 to 6.0	V
Input Voltage	Vin	-0.5 to Vcc+0.5	V
Operating Temperature Range	Ta	0 to +75	℃
Storage Temperature Range	Tstg	-25 to +85	℃

Table 2: Absolute Maximum Ratings

4.2 AC Characteristics

VCC=3.0V, Ta=25℃ unless otherwise noted.

Parameters	Symbol	Minimum	Typical	Maximum
Operating Frequency(RC Oscillator)	Fsys	7.946MHz	8.192 MHz	8.43MHz
RC reset time-constant	Trrc	-	10 us	-
Data ROM data ready time	Tdrr	-	-	2/Fsys

Table 3: AC Characteristics

TEL: +86-0755-27595155 27595165
FAX: +86-0755-27594792
WEB:Http://www.ChipSourceTek.com
E-mail: Sales@ChipSourceTek.com Tony.Wang@ChipSourceTek.com

4.3 DC Characteristics

VCC=3.0V, Ta=25℃ unless otherwise noted.

Parameters	Symbol	Minimum	Typical	Maximum	Condition

PROM address	Function description
0x000 ~ 0x001	Reset
0x004 ~ 0x005	Wake-up
0x008 ~ 0x009	Interrupt
0x00A ~ 0xEFF	User code
0xF00 ~ 0xFFF	Reserve area

Table 3: Memory Map of PROM

5.2 Data ROM (DROM)

The DROM is an OTP (One Time Programmable) type memory. The maximum **DROM is 18K*8-bits** which stores the 8-bits wide data for ADPCM or melody data …etc. The last 64 location is a reserved area. The user shall not use this area in any case. Assembler shall check user data ROM on this limit. Hardware does not need to check this restriction.

DROM address (DMA)	Function description
0x0000 ~ 0x00FF	User area
0x0100 ~ 0x01FF	User area
0x0200 ~ 0x02FF	User area
…	…
0x47B0 ~ 0x47BF	User area (Max. size of TRSP5006A)
0x47C0 ~ 0x47FF	System area, last 64 location(don't use it)

Table 4: Memory Map of DROM

DROM is addressed by four registers DMA3, DMA2, DMA1 and DMA0. After these registers are specified by software, the data need enough delay time, Tdrr in the table of "AC Characteristics". After this delay time, the data can be read from data register (DMDL & DMDH).

Ex:

```
        LD      (DMA0), A
        …
        LD      (DMA3), A       ; Set DMA0~3
        LD      A, (DMDL)       ; Read low nibble data from DROM, address as DMA3~0.
        LD      A, (DMDH)       ; Read high nibble data from DROM, address as DMA3~0.
```

Symbol	Addr	R/W type	Reset	D3	D2	D1	D0	Description
DMA0	18H	R/W	xxxx	DMA0.3	DMA0.2	DMA0.1	DMA0.0	DMA0~3, four register built a 16-bits addressing space for read DROM 8-bits data. DMA0 is lowest nibble, DMA3 is highest nibble of DROM address.
DMA1	19H	R/W	xxxx	DMA1.3	DMA1.2	DMA1.1	DMA1.0	
DMA2	1AH	R/W	xxxx	DMA2.3	DMA2.2	DMA2.1	DMA2.0	
DMA3	1BH	R/W	xxxx	DMA3.3	DMA3.2	DMA3.1	DMA3.0	
DMDL	1CH	R/W	xxxx	DMDL.3	DMDL.2	DMDL.1	DMDL.0	Low nibble of DROM data read from this address.
DMDH	1DH	R/W	xxxx	DMDH.3	DMDH.2	DMDH.1	DMDH.0	High nibble of DROM data read from this address. Write this register means reset watch dog timer if this timer is enabled by option.

Table 5: SFRs about DROM

5.3 SRAM and Special Function Register

5.3.1 SRAM

There are 64 nibbles SRAM in this chip. The SRAM and I/O memory map is divided into several pages by setting MAH register (1-bit wide). The initial value of MAH is unknown and must be defined by instructions "LDMAH" before you utilize SRAM. The extra 2 SRAM nibbles in the specifications and hardware manuals of relative mask ROM products are not SRAM in fact. They are USER1 and USER2 of SFRs.

Direct Addressing		SRAM MAP
MAH=XH	00H~1FH	SFR(special function register) register
MAH=0H	20H~3FH	USER SRAM
MAH=1H	20H~3FH	

Table 6: Memory Map of SFRs

The first 32-nibble, 00H ~ 1FH, are defined as a common block. Some I/O and user register is arranged in this common block for easy data operations. The other regions, 20H~3FH, are employed as SRAM.
The user must notice that the initial content of SRAM is unknown.

5.3.2 Special Function Registers

The special function register consists of common I/O and other special register.
A special function register supports LD/ADC/SBC/OR/AND/XOR/INC/DEC/RLC/RRC/CMP/ADR operation. Bit set/clear can only be operated on the address range from 00H to 0FH, except indirect operation is used.
The following table describes all of the SFRs.

Symbol	Addr	R/W type	Reset	D3	D2	D1	D0	Description
STATUS	00H	R/W	00xx	reserved	PWFG	CF	ZF	Status Register PWFG: PWM interrupt flP

AUD_DH	0BH	W	xxxx	AUD_DH3	AUD_DH2	AUD_DH1	AUD_DH0	AUD_DH[3:0]: The high nibble of 8 bits PWM. The bit9~6 of 10 bits PWM. The bit11~8 of 12 bits PWM. Note: AUD_DH3 is sign bit, “0” means positive.
Reserved	0CH~ 0EH	-	xxxx	-	-	-	-	Reserved
USER2	0FH	R/W	xxxx	USER2.3	USER2.2	USER2.1	USER2.0	General purpose user register.
IADJ	10H	R/W	0000	CMPSEL1	CMPSEL0	ADJ1	ADJ0	CMPSEL[1:0]: Enable option PCEIO, ENOP, ENCMP1, and set ENGAIN=1, Select Gain in record mode. CMPSEL[1:0] / GAIN: 00 / 50; 01 / 100; 10 / 150; 11 / 200 ADJ[1:0]: Adjust the frequency, when enable option OTPADJ. ADJ[1:0] / Frequency %: 00 / -4%; 01 / -2%; 10 / 2%; 11 / 4%
CNTI	11H	R/W	0000	ENGAIN	-	S2S	-	ENGAIN: 1: Open Built-in gain in record mode. 0: Close Built-in gain in record mode. S2S: PWM input Data format 1: 2's format 0: sign **Notice: If ENGAIN enabled, option OPEN function should be disable.**
PWMWK	12H	R/W	0000	PWMWKFG	CLAPSEL1	CLAPSEL0	PWMWKEN	PWMWKFG： When wakeup source form Speaker, it will be set by hardware, it could be clear by software. PWMWKEN: Wakeup by speaker. 1: Enable PWM wakeup function. 0: Disable PWM wakeup function. CLAPSEL[1:0]: Sensitivity of speaker wakeup. CLAPSEL[1:0] / Sensitivity: 00 / Level 1 (low); 01 / Level 2; 10 / Level 3; 11 / Level 4 (High)
LVD_CTRL	13H	R/W	0000	-	-	LVD_FLAG (R)	LVDEN	LVD_FLAG: (Read only) The flag of LVD, '1'=LVD sensing. LVDEN: '1'=Enable LVD function, '0'=Disable LVD function.
LVDS	14H	R/W	0000	LVDS3	LVDS2	LVDS1	LVDS0	LVDS[3:0]: LVD level selected, 1111=3.8V, 1110=3.7V, 1101=3.6V, 1100=3.4V, 1011=3.3V, 1010=3.2V, 1001=3.1V, 1000=3.0V, 0111=2.9V, 0110=2.8V, 0101=2.7V, 0100=2.5V, 0011=2.4V, 0010=2.3V, 0001=2.2V, 0000=2.1V.
Reserved	15H~ 17H	-	xxxx	-	-	-	-	Reserved
DMA0	18H	R/W	xxxx	DMA0.3	DMA0.2	DMA0.1	DMA0.0	DMA0~3, four register built a 16-bits addressing space for read DROM 8-bits data, DMA0 is
DMA1	19H	R/W	xxxx	DMA1.3	DMA1.2	DMA1.1	DMA1.0	

DMA2	1AH	R/W	xxxx	DMA2.3	DMA2.2	DMA2.1	DMA2.0	lowest nibble, DMA3 is highest nibble of DROM address.
DMA3	1BH	R/W	xxxx	DMA3.3	DMA3.2	DMA3.1	DMA3.0	
DMDL	1CH	R/W	xxxx	DMDL.3	DMDL.2	DMDL.1	DMDL.0	Low nibble of DROM data read from this address.
DMDH	1DH	R/W	xxxx	DMDH.3	DMDH.2	DMDH.1	DMDH.0	High nibble of DROM data read from this address. Writing this register means reset watch dog timer if this timer is enabled by option.
Reserved	1EH~ 1FH	-	xxxx	-	-	-	-	Reserved

Table 7: All of the Special Function Registers

5.4 Interrupt Vector Address

Vector	Address
RESET	00H
WAKEUP	04H
INT	08H

Table 8: Interrupt Vectors

5.5 Interrupt Controller

There is only one interrupt entry point in this chip. Normally interrupt period is 32768Hz. It can be changed to 65536Hz by option “PWM64K”. Program will jump to address 0x008 when an interrupt occurs.

Symbol	Addr	R/W type	Reset	D3	D2	D1	D0	Description
STATUS	00H	R/W	00xx	reserved	**PWFG**	CF	ZF	Status Register **PWFG:** PWM interrupt flag. CF: Carry flag. ZF: Zero flag.
PWM_CTRL	09H	R/W	--x0	reserved	reserved	**ENINT**	**ENPWM**	**ENPWM:** “1” Enable PWM, “0” Disable PWM. **ENINT:** Enable global interrupt.

Table 9: SFRs about Interrupt

If the global interrupt enable bit (INTEN) is high and interrupt request (PWFG=1) occurred, then interrupt will be accepted on next clock. On that instant, current (next) program counter, PCDH, MAH and C/Z will be stored in special hardware registers, and program counter will be loaded with entry address of that interrupt. All these are done in one clock. Interrupt enable bit will be cleared too. As long as program enters interrupt service, interrupt enable bit is cleared. It's no need to clear interrupt enable flag in interrupt routine. But hardware will not clear interrupt request flag (PWFG). Software is required to clear it.

When interrupt service routine is done, an RETI shall be executed. This instruction will restore stored program counter, PCDH, MAH and C/Z, will set interrupt enable bit=1 also. (Note that RETI is different from RETS.) Interrupt request can be accepted only when enable bit be set. Note that only one level of INT routine can be used.

5.6 Clock Operation

There are two operation modes in this chip. The state diagram of three MCU operation modes is shown below:

1. NORMAL Mode: In normal mode, system clock oscillator is running, and MCU clock source is come from main oscillator. In NORMAL mode, MCU will go to halt mode after HALT instruction executed.

2. HALT Mode: In HALT mode, the MCU clock stops, users can't change the operation mode when in halt mode. It will go back to NORMAL mode (Program counter=0x004) when I/O wakeup or reset occurred. Please refer to the section of" Halt Mode & Wake up" for the detailed HALT mode description.

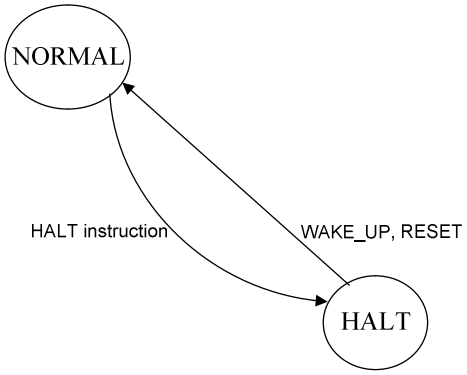


Figure 2: Clock Operation Mode

5.7 Halt Mode & Wake up

The MCU is changed into HALT mode (program counter and system clock stop) when HALT instruction executed. It provides a power saving mode for those applications requiring a very low stand-by current. The PA[3:0] are supporting the wake-up function when rising edge occurred.

The program counter will be 0x004 when HALT instruction executed immediately, then program counter will go to next address after 64 stable clock(system clock) when wake up condition occurred. Reset signal will release HALT state and execute reset procedure because reset is first priority when in HALT mode, so program counter will from 0x004 to 0x000, program counter goes to next address after 64 stable clock cycles. Furthermore, the SRAM will keep their previous data without changing in this mode.

5.8 Watch Dog Timer Reset (WDT)

The **Watch Dog Timer (WDT)** is used to reset whole chip when detect unexpected execution sequence caused by accident condition, avoiding dead lock of MCU program. WDT will be reset when wake-up from halt, after reset or software clears it. The watch dog timer is a simple counter. It has a fixed length of **256*256*16/system-clock (ex: 0.13 sec for 8.192MHz system clock)** after the clearance of watch dog.

Software must run a "clear watch dog timer" (write to DMDH) instruction before this timer time out when WDT enabled. It will generate a reset signal to reset whole system when WDT over flow. Assembler will check user program about the "reset watch dog" instructions. If more than one "reset watch dog" is found in program, assembler will generate a warning (program code will still be generated). "HALT" instruction will reset watch dog timer. The reset watch dog timer sequence is strongly recommended as:

```
WATCHDOG:
        LD      (1DH), A
```

5.9 Low Voltage Detect (LVD)

The low voltage detect (LVD) function is used to detect whole chip power supply VCC. TRSP5006A support 16-level LVDS[3:0] to selected detect voltage level, the detected voltage range is from 3.8V to 2.1V.

There have one control register LVDEN used to enable/disable the low voltage detect function. The flag signal LVD_FLAG is used to check the power supply VCC upper or under than low voltage detect level, when VCC upper than LVD level, the flag LVD_FLAG value is low; otherwise, the flag LVD_FALG value is high when VCC under than VCC.

Symbol	Addr	R/W type	Reset	D3	D2	D1	D0	Description
LVD_CTRL	13H	R/W	0000	-	-	**LVD_FLAG (R)**	**LVDEN**	**LVD_FLAG: (Read only)** The flag of LVD, '1'=LVD sensing. **LVDEN:** '1'=Enable LVD function, '0'=Disable LVD function.
LVDS	14H	R/W	0000	**LVDS3**	**LVDS2**	**LVDS1**	**LVDS0**	**LVDS[3:0]:** LVD level selected, 1111=3.8V, 1110=3.7V, 1101=3.6V, 1100=3.4V, 1011=3.3V, 1010=3.2V, 1001=3.1V, 1000=3.0V, 0111=2.9V, 0110=2.8V, 0101=2.7V, 0100=2.5V, 0011=2.4V, 0010=2.3V, 0001=2.2V, 0000=2.1V.

5.10 8/10/12 Bits PWM/DAC

There are three optional PWM/DAC output resolutions. One is 8-bits output, the sec. is 10-bits output, and the other is 12-bits output. The highest of input data is signed bit: ‘0’ represents positive, ‘1’ represents negative.

TRSP5006A supports audio output with PWM and DAC two modes. These two modes can be selected by “DACEN” option. If use DAC output mode, option “DACEN” must be enabled. Otherwise, PWM mode is enabled. All PWM registers will be exchanged for DAC mode if “DACEN” option is enabled.

Symbol	Addr	R/W type	Reset	D3	D2	D1	D0	Description
STATUS	00H	R/W	00xx	reserved	**PWFG**	CF	ZF	Status Register **PWFG:** PWM interrupt flag. CF: Carry flag. ZF: Zero flag.
AUD_DLL	08H	W	xxxx	**AUD_DLL3**	**AUD_DLL2**	**AUD_DLL1**	**AUD_DLL0**	**AUD_DLL[3:2]:** The bit1~0 of 10-bits PWM, combine with AUD_DL[3:0], AUD_DH[3:0] to built 10-bits PWM if option PWM10 is 1 and PWM12 is 0. **AUD_DLL[3:0]:** The bit3~0 of 12-bits PWM, combine with AUD_DL[3:0], AUD_DH[3:0] to built 12-bits PWM if option PWM12 is 1.
PWM_CTRL	09H	R/W	--x0	reserved	reserved	**ENINT**	**ENPWM**	**ENPWM:** “1” Enable PWM, “0” Disable PWM. **ENINT:** Enable global interrupt.
AUD_DL	0AH	W	xxxx	**AUD_DL3**	**AUD_DL2**	**AUD_DL1**	**AUD_DL0**	**AUD_DL[3:0]:** The low nibble of 8-bits PWM. The bit5~2 of 10-bits PWM. The bit7~4 of 12-bits PWM.
AUD_DH	0BH	W	xxxx	**AUD_DH3**	**AUD_DH2**	**AUD_DH1**	**AUD_DH0**	**AUD_DH[3:0]:** The high nibble of 8 bits PWM. The bit9~6 of 10 bits PWM. The bit11~8 of 12 bits PWM. Note: AUD_DH3 is sign bit, “0” means positive.

Table 10: SFRs about the operation of PWM

5.10.1 8-Bits PWM/DAC

This PWM is 8-bits output resolution. An interrupt request happened when a PWM cycle completed.

The MSB of AUD_DH is signed bit, '0' for positive, '1' for negative. PWM output frequency (sample rate) is fixed at 32KHz. PWM data registers are AUD_DL, AUD_DH. The AUL_DL is low nibble (D3 ~ D0). AUD_DH is high nibble (D7 ~ D4). D7 is the signed bit and D6 ~ D0 is the length (clock number) of output active pulse. Software should write AUD_DL and AUD_DH before enable PWM.

When an interrupt request happened, PWM interrupt flag bit PWFG of STATUS register will be "1". The PWM will load previously-written-data into actual conversion port on end of a PWM code output. So program can write data into PWM data store safely at beginning of an interrupt service routine. (A PWM interrupt means PWM data loaded, next data is expected). This timing shall be controlled carefully such that data writing in the beginning of interrupt service routine is safe. If data is not changed during a conversion, previous data will be used.

This PWM output can drive 8 ohm speaker. PWM can be enabled or disabled by setting/clearing ENPWM of PWM_CTRL. When disabled, the PWMP, PWMN pins are all '0'. "HALT" instruction will disable PWM (clear ENPWM of PWM_CTRL) and the PWMP and PWMN pins will be tri-state.

5.10.2 10-Bits PWM/DAC

The frequency of PWM clock is fixed at 32 KHz if 10-bits PWM mode is selected by option. The 10-bits PWM data (AUD_DH[3:0], AUD_DL[3:0], AUD_DLL[3:2]) are consist of AUD_DH, AUD_DL, AUD_DLL three registers shown above. The data rage is 0 ~511. Software should write these registers before PWM is enabled. The other features of 10-bits PWM is the same as 8-bits PWM.

5.10.3 12-Bits PWM/DAC

The frequency of PWM clock is fixed at 32 KHz if 12-bits PWM mode is selected by option "PWM12S". The 12-bits PWM data (AUD_DH[3:0], AUD_DL[3:0], AUD_DLL[3:0]) are consist of AUD_DH, AUD_DL, AUD_DLL three registers shown above. The data rage is 0 ~ 2047. Software should write these registers before PWM is enabled. The other features of 12-bits PWM is the same as 8-bits PWM.
Note: To avoid sound "Bo", please reference application note on web site.

5.10.4 Speaker Provided a Wake-up Control Function

Normally, the PWMN and PWMP pin is tied to a speaker for playing music and a sound. This speaker connection structure can be used to wake-up MCU. If PWMWK is enabled, the speaker wake-up function is enabled after go into HALT mode and the PWM function keep operating in normal mode. If speaker wake-up function is enabled, the PWMP pin will be fixed to VSS level and PWMN pin also will be fixed to VSS level by chip.

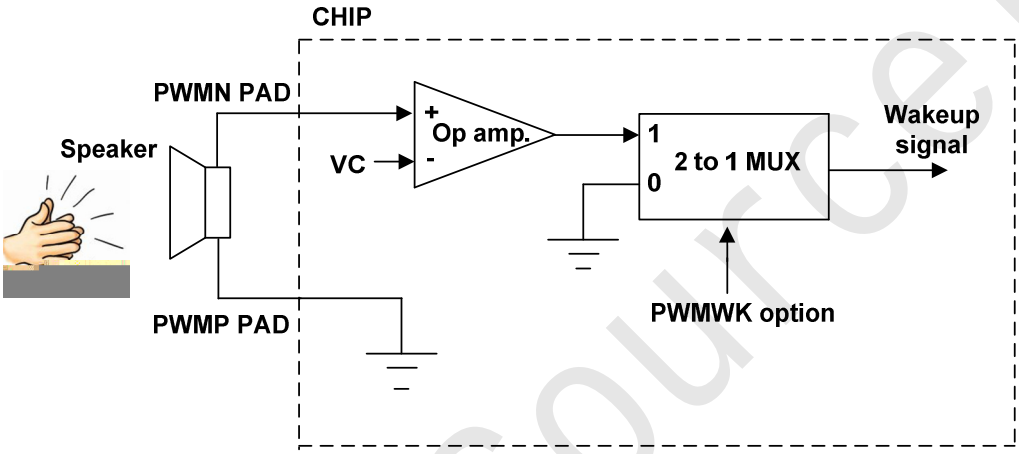
The signal level on PWMN pin will be changed (typically 0mV~10mV) when a sound receives from speaker. The MCU will be waked up if signal level on PWMN pin high enough. The relationship between wake-up signal and PWMN pin is shown in picture below. The wake-up signal goes high if PWMN pin larger than VC level and it goes low if PWMN pin smaller than VC level.

Note:
1. This function consume about 5uA (VDD=5V) typically in HALT mode when "PWMWK" option is enabled.
2. PWM function must be keep silence about 200ms before go into HALT mode. Otherwise, MCU maybe keep in normal mode, not goes into HALT mode.
3. When PWMWK option enabled, PA0 wakeup option must be disabled, please referenced AN-0068_V2.0.
4. If ENGAIN enabled, option OPEN function should be disable.

Symbol	Addr	R/W type	Reset	D3	D2	D1	D0	Description
PWMWK	12H	R/W	0000	PWMWKFG	CLAPSEL1	CLAPSEL0	PWMWKEN	**PWMWKFG** : When wakeup source form Speaker, it will be set by hardware, it could be clear by software. **PWMWKEN:** Wakeup by speaker. 1: Enable PWM wakeup function. 0: Disable PWM wakeup function. **CLAPSEL[1:0]:** Sensitivity of speaker wakeup.

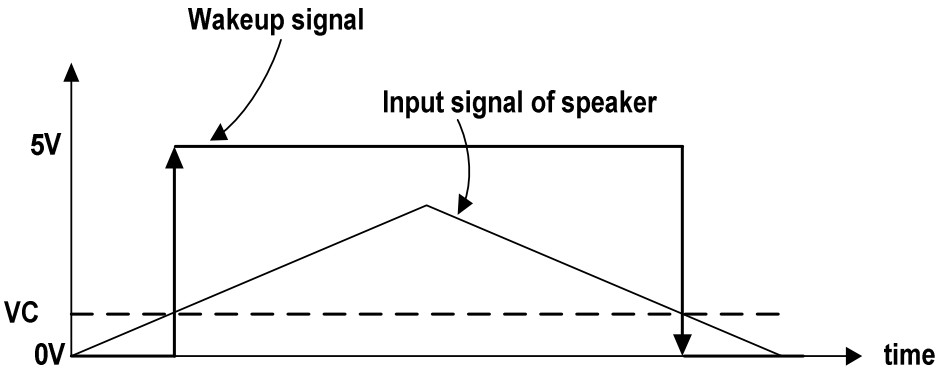
CLAPSEL[1:0]	Sensitivity
00	Level 1 (low)
01	Level 2
10	Level 3
11	Level 4 (High)

Table 13: SFRs about the operation of speaker wakeup function



Wakeup control block diagram and speaker trigger application circuit

Figure 3: Speaker wakeup structure



Input signal of speaker vs. Wakeup signal waveform

Figure 4: Speaker wakeup waveform

Notice: Speaker wakeup function, please reference application note "AN-0068_V1.0" on web site.

5.11 Reset Function

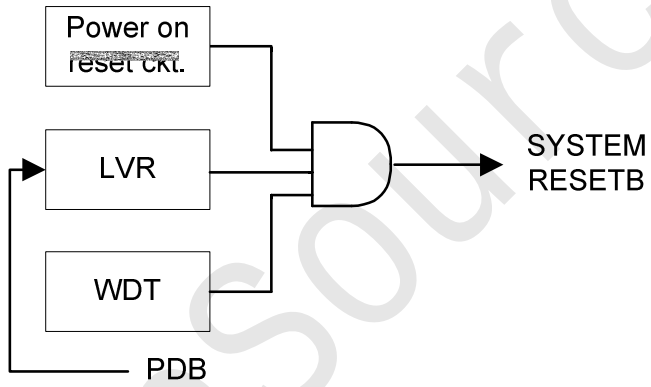


Figure 5: Reset structure

The system reset is come from three signals which are **Power on reset**, **Low voltage reset(LVR)** and **WDT overflow reset**.

For normal operation of this chip, a good reset is needed. The operation frequency of MCU will go back to normal mode when reset occurred in HALT mode.

5.12 System Clock Oscillator

This chip MCU is typically operated on 8.192MHz which is generated from internal RC oscillator 32MHz.

5.13 I/O Ports

There is one I/O port PA3~PA0, whose input/output direction are defined by IOC_PA. The wake-up functions of PA3~PA0 are enabled or disabled by option. All I/O ports provides rising or falling edge wake up function. This double edge wake up function can be enabled by "BIWK" option. Their 1M/50K Ohm pull down resistors are optional.

In order to achieve touch function, TRSP(M)5018A support 220K Ohm pull down resistors. These resistors can be enabled by using 50K Ohm pull down resistor registers after "PD220K" is enabled. The 220K Ohm resistance value is almost fixed value when VCC change from 2.0V to 5.5V.

5.13.1 Port PA (input/output)

The Port A is 4-bits bidirectional I/O port. Their directions can be defined by IOC_PA bit by bit.
The following table describe the SFRs associated with Port A.

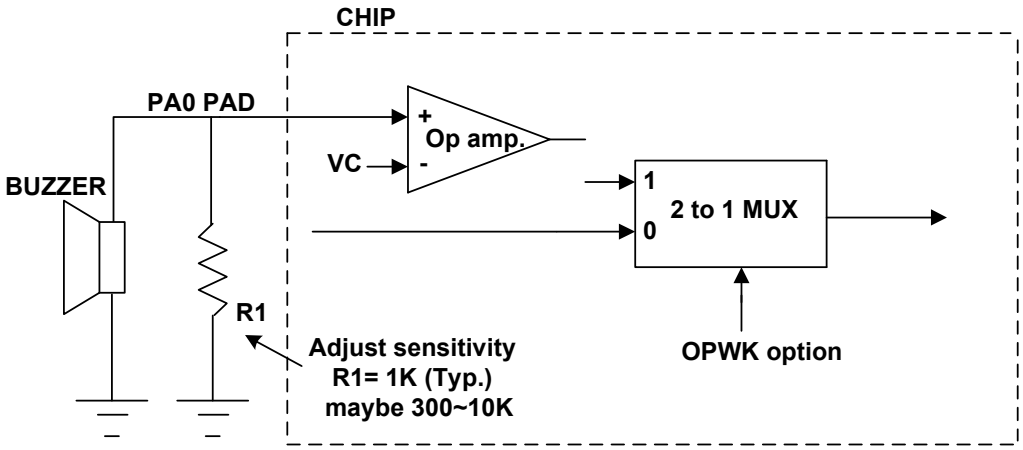
Symbol	Addr	R/W type	Reset	D3	D2	D1	D0	Description
IOC_PA	02H	R/W	0000	**IOCA3**	**IOCA2**	**IOCA1**	**IOCA0**	**"1" = output, "0" = input of related PA bit.**
DATA_PA	03H	R/W	xxxx	**DPA3**	**DPA2**	**DPA1**	**DPA0**	**Read from Port A input port and write to output port.**

Table 14: SFRs of Ports PA

In output mode, the data can be written out to external pin, and reading this output port will read the data internal latch. Pull-down resistor will be disabled when output mode is selected.
In input mode, Port A data can be read from external pin, and they are attached with 1M/50K Ohm pull-down resistor or not according to the options.

In addition, each pin of Port A also can be accompanied with wake-up function according to the options. In HALT mode, if some bits of Port A are accompanied with wake-up function, any rising edge occurred on that pin will wake up system and turn on oscillator, and the program counter of MCU will jump to the address 0x004. This device will start to execute the wake-up sub-routing.

PA3 is provided with 38KHz m68 0 Td [( )-11.3(")-4.6(B)3.9..4(k)-cT -222.977 733 0 0 cm BT /F3 9 Tf .999w3pro222.25



PA0 analog wakeup block diagram and buzzer trigger application circuit

6. TRSP5006A The Application Circuit

7. TRSP5006A Option Registers table

Option Name	Function Description
BZWK	PA0 buzzer trigger wakeup
RCWK	PA0 RC wakeup
PWM64K	PWM int. freq. select
DACEN	DAC function control
WAKEBA	Wake-up enable for PA3~PA0 respectively
PD50KPA	50K Ohm pull down resistor for PA3~PA0 respectively.
PD1MPA	1M Ohm pull down resistor for PA3~PA0 respectively.
WDGENB	Watch dog timer
HALTENB	HALT mode control
PD220K	Change 50K Ohm pull-down resistor to 220K Ohm
PWM12S	PWM 12 bit select
PWM10S	PWM 10/8 bit select
OTPLOCK	Security control
F38K	PA3 38KHz output
BIWK	Bi-directional wake up
OPTADJ	OSC IADJ select
HDEN	Driving capacity of output port control

8. TRSP5006A The Revision History

Version	Description	Page	Date
1.0	Established		2021-01-04

Table 15: Revision History